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Paper

Two-step Poly-Si Through-silicon via for High-temperature Process of Bioprobe

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TSV (Through-Silicon Via) is a technology, which realizes an electrical connection from the surface to the backside of the silicon (Si) substrate, offering advantages of device minimization for bioprobe applications. To realize the TSV, copper (Cu) has widely been used as the via material. However, Cu cannot be used for a high temperature process (e.g., 700°C for Si growth process). To realize TSVs for high temperature processes, here we propose a poly-Si–based 'two-step TSV', which consists of different hole sizes at the surface and bottom of the Si substrate. By utilizing deep reactive-ion etching (RIE), a 50-μm-diameter and 240-μm-depth hole was formed on the backside of the substrate, while a 12-μm-diameter and 10-μm-depth one was formed on the surface side of the substrate with the same alignment. The TSV is then filled with heavily-doped poly-Si, which is simultaneously deposited in the process of Si_2H_6 gas-based vapor-liquid-solid (VLS) growth of Si-microneedles. The current-voltage characteristics of the fabricated TSV show a linear behavior with a resistance of 6 kΩ, confirming the feasibility of the proposed TSV.

Keywords : through-silicon via (TSV), poly-Si, bioprobe, VLS growth

1. Introduction

TSV[(1)-(4)] is a technology, which realizes an electrical connection from the surface to the backside of the Si substrate. The TSV includes several advantages of miniaturization, high-densification, and multi-terminal of the device. Taking these advantages of the TSV, bio-signal recording needle-electrode arrays with vertical multiple electrical connections within a small device's geometry, can be realized.

For the bioprobe application, we have proposed vertically aligned high-density Si-microwires on a Si substrate by VLS growth at a growth temperature of > 700°C[(5)(6)]. However, surface-sided device interconnections cause device issues, including a low density of the electrode array and increase in the area of the device substrate (e.g., > 8 mm × 3 mm for 11ch electrode device[(7)]). The next step of our Si-microwire–based bioprobe device is to be fabricated on the TSV substrate for the device minimization (e.g., < 1 × 1 mm^2) with a high array density (e. g., ~ 100 μm in pitch).

To realize TSV, copper (Cu) as the via material has been used. However, Cu can not be used for a high temperature process (e.g., 700°C for VLS growth). In addition, the thermally diffused Cu into the Si substrate changes the properties of the devices (e.g., electrical properties of Si-MOSFET). To avoid this process issue, instead of the use of Cu, an Si–based TSV has been proposed[(4)]. However, fabricating the Si-TSV with a high aspect ratio is still problematic. The other issue of the Si-TSV is the insulation of such a high-aspect-ratio TSV by filling the trench with silicon dioxide (SiO_2).

To realize TSVs for high temperature processes, here we propose a poly-Si–based 'two-step TSV' (Fig. 1), in which the inside of the via hole is covered with heavily-doped poly-Si for the electrical connection from the surface to the backside of the substrate. In addition, the TSV consists of different hole sizes at the surface and bottom of the Si substrate, realizing the minimization of the TSV-hole at the device surface (< 10 μm in diameter).

With a conventional TSV process, in order to fabricate an < 10 μm diameter via hole for a thick Si-substrate (e.g., > 250 μm in thickness), the via hole should be formed with a high aspect ratio (Fig. 2). Our proposed two-step TSV solves this process issue by fabricating holes from both sides of the substrate (top and back sides) with the different diameters. The TSV process includes two advantages; i) reduction of hole-size (e.g., < 10 μm in diameter) at the device side and ii) small amount of poly-Si for filling the hole. In addition, due to the material of poly-Si, the TSV is simultaneously formed in the process of Si_2H_6 gas–based VLS growth of Si-microneedles.

2. Fabrication Process

The process starts with a 250-μm-thick (111)-Si wafer, which has a thermal oxide layer (~1 μm-thick). To form a via hole from the substrate backside, the SiO_2 on the backside was patterned with the diameter of ~50 μm, and then substrate was etched by Deep RIE. The same process was repeated on the surface side with the diameter of ~10 μm (Fig. 3 (a)). After the via formation, the substrate was thermally oxidized to form SiO_2 (0.5 μm-thick) inside the via for the substrate insulation. Pt electrode at the backside of the substrate for the electrical connection was formed

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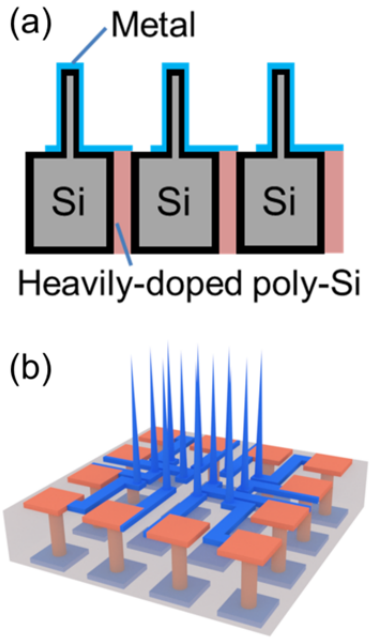

Fig. 1. Poly-Si–based 'two-step TSV' for bioprobe array device. (a) A cross-sectional view of vertical needle-electrode with the TSVs. (b) Schematic of the proposed bioprobe array device. Taking advantages of the TSV, bioprobe devices with multiple electrical connections within a small device's geometry can be realized.

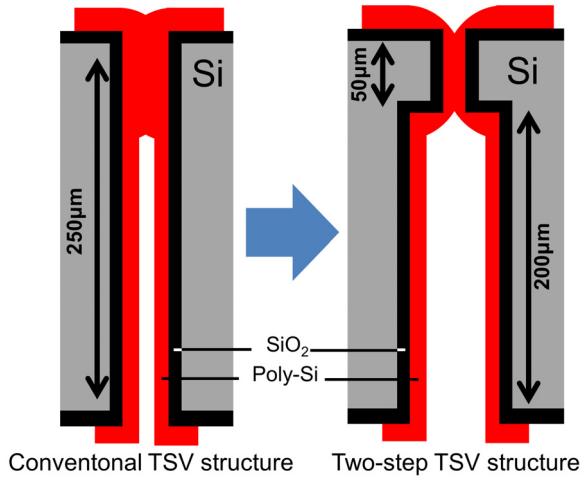

Fig. 2. Geometrical comparison of TSV structure between conventional and proposed 'two-step'. Depths of top-hole (50 μm) and bottom-hole (200 μm) are design values.

by sputtering and lift-off processes. To form the Si microneedle by gold (Au)-catalyzed VLS growth with the Si gas source [a mixture gas of 1% phosphine (PH_3) diluted in 99% hydrogen as a dopant gas and 100% disilane (Si_2H_6) as source gas for the Si needle growth][6], Si substrate was exposed by patterning the SiO_2 layer. At the exposed Si substrate, an Au dot for the VLS growth was placed by evaporation and lift-off. With a 200-nm-thick and 6-μm-diameter Au pattern, a 200-μm-long Si-microneedle with a 10 μm diameter was formed by the VLS growth. Simultaneously,

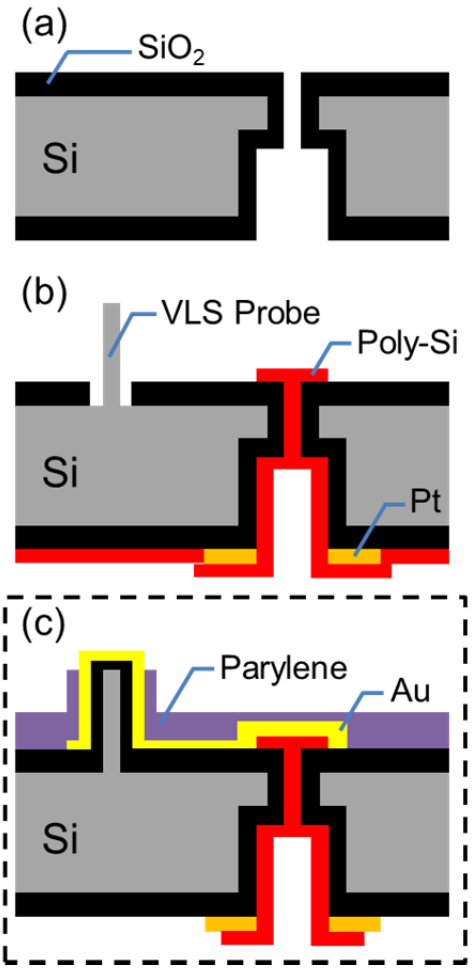

Fig. 3. Fabrication process steps of two-step poly-Si TSV. (a) Fabrication of the via-hole and thermal oxidation. (b) Simultaneous poly-Si fill and Si-microneedle growth by Si_2H_6 gas–based VLS growth. (c) Device metallization (e.g., Au) and encapsulation (e.g., parylene) (data not shown in this paper).

the poly-Si deposits inside the via hole during the VLS growth, resulting in the electrical connection from the surface to the backside of the substrate via the conductive poly-Si. Poly-Si at the surface side of the substrate was patterned by RIE with photoresist mask (Fig. 3 (b)). For the poly-Si patterning at the device backside, we use XeF_2 etching with photoresist mask (Fig. 3 (c)).

3. Results

3.1 Fabricated Two-step Poly-Si TSV Figure 4 shows SEM images taken from each process step in the fabrication of the two-step TSV. The first hole, which has the diameter of 50 μm and the depth of 240 μm, was formed on the backside of the substrate by Deep-RIE with SF_6 and C_4F_8 gases (Fig. 4 (a) and (b)) (design values of diameter and depth of the hole were 50 μm and 200 μm, respectively). With the same RIE process, the second hole with the diameter of 12 μm and the depth of 10 μm was formed on the surface of the substrate (Fig. 4 (c)) (design values of diameter and depth of the hole were 10 μm and 50 μm, respectively). Figure 4 (d) shows the SEM image, taken from the backside of the substrate, confirming a smaller hole (2nd RIE) formed inside the larger hole

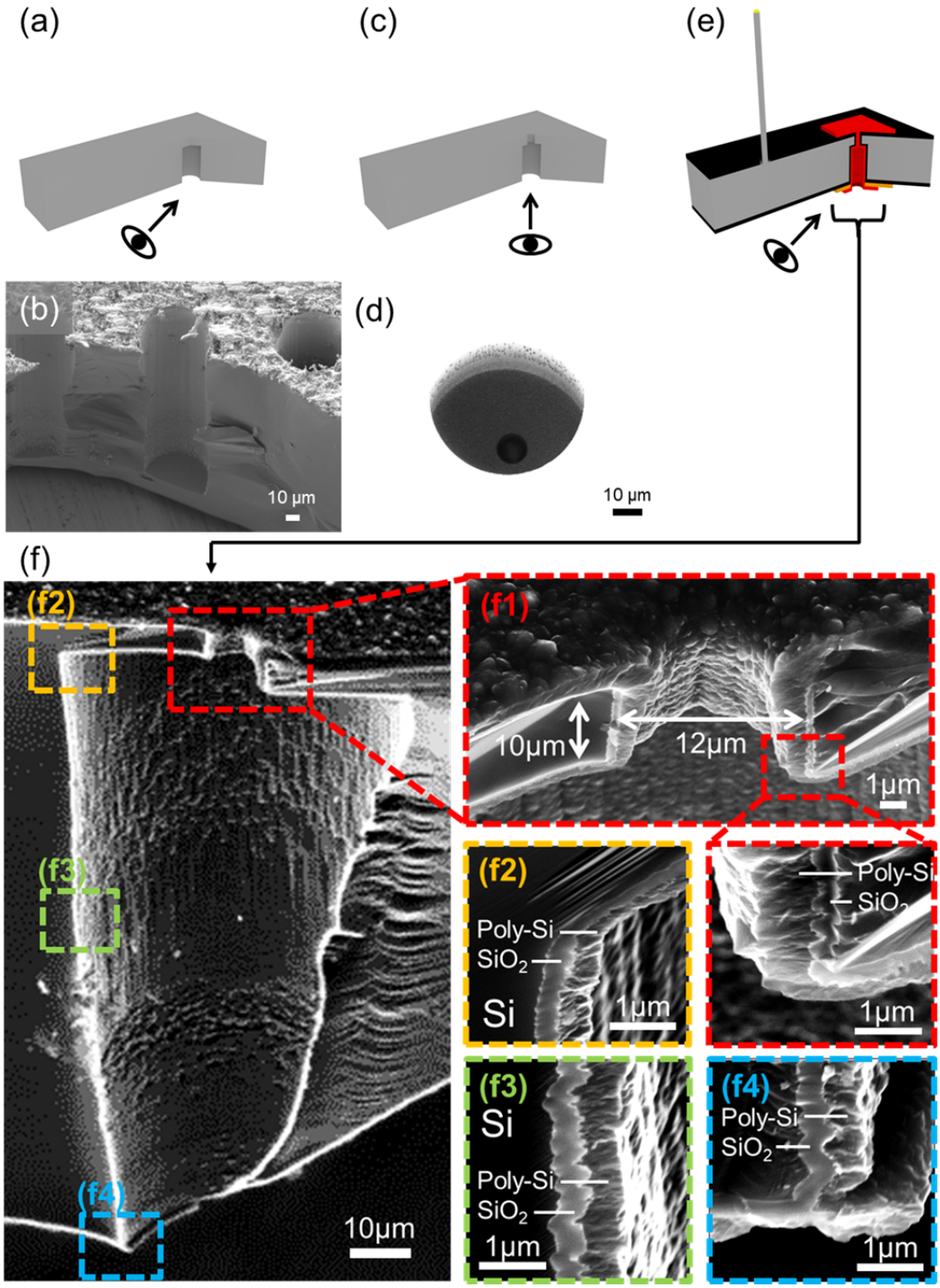

Fig. 4. Schematics and SEM images of each process step, and SEM observations of fabricated two-step poly-Si TSV. (a), (b) Schematic and SEM image of backside hole. (c), (d) Schematic and SEM image of the top-hole. (e), (f) Schematic and SEM image of the two-step TSV after the poly-Si deposition: cross sectional SEM image of the top-hole (f1), cross sectional SEM image at the corner section between the top and the bottom holes (f2), cross sectional SEM image of the sidewall of the bottom-hole (f3), and cross sectional SEM image at the edge of the bottom-hole (f4).

(1st RIE). After forming Pt pad at the backside (sputtering and lift off), the microneedle was formed by VLS growth, while the poly-Si was deposited inside the via hole (Fig. 4 (e)).

Thickness of the poly-Si formed inside the via hole varied, depending on the section of the via hole. Figure 4 (f) shows a set of enlarged SEM images of poly-Si/SiO_2/Si system taken at each section of a via hole. Figure 4 (f1) is the top-hole with the diameter of 12 μm and the depth of 10 μm, showing that the inside of the hole including the edges were covered with the poly-Si layer. The poly-Si layer is observed continuously from the top-hole to the bottom-hole (Fig. 4 (f2)). Figure 4 (f3) shows the middle section of the hole, showing the poly-Si with the thickness

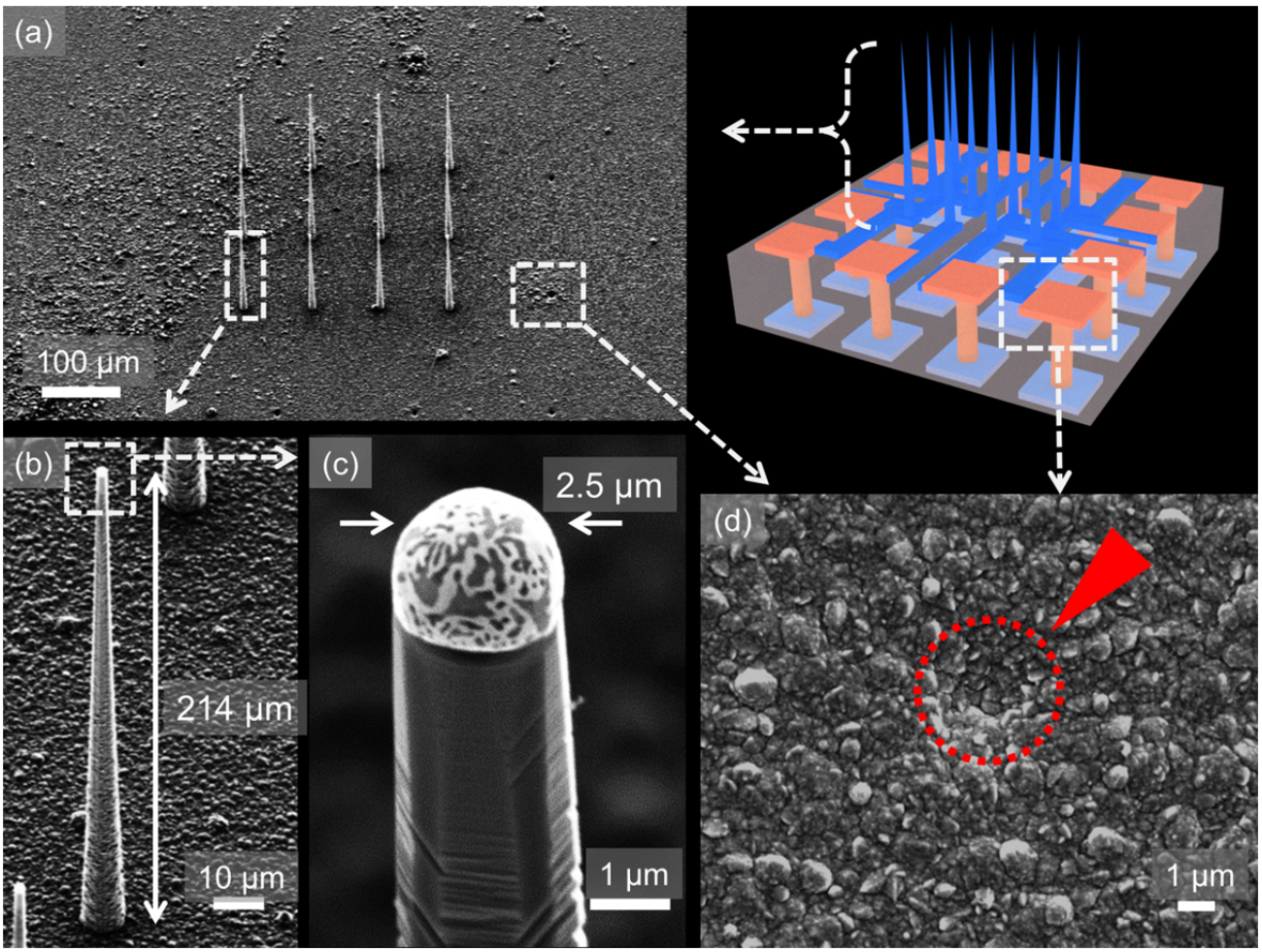

Fig. 5. SEM images of fabricated Si-microneedles. (a) SEM image of a 3 × 4 array of the microneedles. (b) SEM image of a microneedle, with the height of 214 µm. (c) SEM image of the tip-section of the needle. The tip diameter is 2.5 µm. (d) SEM image of the top-hole of a via, showing that the hole is fully filled with poly-Si.

of 0.6 µm. At the bottom-hole, the edge is also covered with the poly-Si layer (Fig. 4 (f4)). Due to the thickness of Pt of 200 nm, Pt-layer between the Poly-Si and back-side substrate (SiO_2) was not observed clearly.

The poly-Si deposition at 720°C also resulted in the VLS growth of Si-microneedle from the catalyzed Au dots. Figure 5 (a) shows an array of 12 microneedles by the VLS growth for the growth time of 180 min. The gaps between these needles are 100 µm and 120 µm, respectively. The length and tip-diameter of each needle were 214 µm and 2.5 µm, respectively (Fig. 5 (b) and (c)). Figure 5 (d) shows the top-via of a TSV, indicating that the via hole is filled with the poly-Si.

3.2 Electrical Properties of Two-step Poly-Si TSV

Figure 6 (a) shows the current-voltage characteristics of the fabricated two-step poly-Si TSV, measured by using a prober station (PM8, SUSS MicroTec, Germany) and a semiconductor parameter analyzer (4200, Keithley Instruments, USA). Herein, a probe of tungsten made contact with the surface-sided contact pad of heavy doped poly-Si (n-type), while the other back-sided contact pad of the poly-Si was in contact with the metal plate of the prober station. Diameters of the top and bottom of the measured via hole are 12 µm and 50 µm respectively. Lengths are 10 µm for the top hole and 240 µm for the bottom hole. Current-voltage characteristics of the TSV show the linear behavior with the resistance of 6 kΩ.

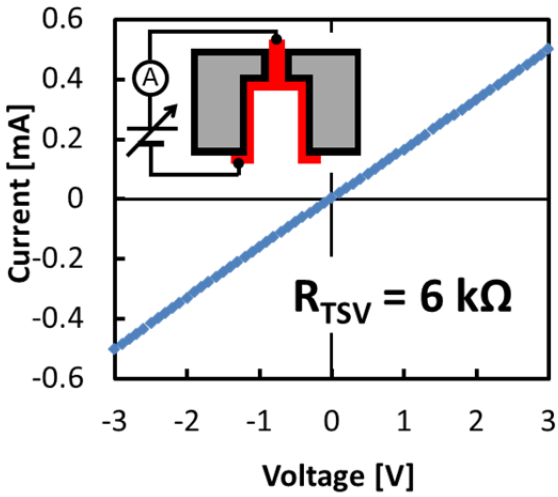

Fig. 6. Current-voltage characteristics of fabricated two-step poly-Si TSV.

4. Discussion

To achieve an array of microneedles for bioprobe application, we fabricated two-step poly-Si TSVs, with a measured resistance of 6 kΩ. The resistance was not consistent with the theoretical value of 643 Ω, which is obtained by using the poly-Si resistivity of 0.02 Ωcm (experimentally measured value) and the TSV's geometry. The reason of the resistance inconsistency is probably due to the uniformity of the thickness of poly-Si. The theoretical resistance of TSV is calculated by assuming a uniform thickness of the poly-Si of 0.6 µm. However, the thickness of the poly-Si formed inside the via hole varied, depending on the section of the via hole, as confirmed in the SEM observations (Fig. 4 (f)). Figure 4 (f2) shows the middle portion of the via hole, showing the thinnest poly-Si in the TSV system. Such thin poly-Si sections dominate the overall resistance of the whole TSV system (6 kΩ).

The thickness of poly-Si depended on the substrate temperature. Figure 4 (f1) shows the top-hole of a TSV, which is not fully filled with the poly-Si. These TSVs were observed at the edge on the Si substrate. Herein, the substrate used in the poly-Si deposition (VLS growth) was two inch Si-wafer, which was heated at 720°C with a resistive heater. On the other hand, although the same parameters of process gas (PH_3 and Si_2H_6) were used, we observed a fully filled top-hole of the TSV at the center portion in the Si wafer, due to the temperature of the wafer center portion being higher than that of the edge. To form fully filled top-holes with the poly-Si in the entire wafer, one way is to use a smaller diameter for top-holes (e.g., 2 µm) located at the wafer edge. The other way is to heat the wafer uniformly, by using a several zoned heater system for the graded heating (higher temperature for the wafer-edge and lower temperature for the wafer-center).

We demonstrated the fabrication of two-step poly-Si TSVs for a high-density Si-microneedle array device. For the device completion, additional processes including device metallization for both needles and device interconnections are necessary[7][8]. The metallization can be realized by metal sputtering (e.g., Au with a binding layer of titanium). After the device metallization, the sidewall of each microneedle and device interconnection can be insulated by forming an insulator (e.g., biocompatible layer of parylene-C), while the tip-section of the needles is exposed (Fig. 3 (c)).

5. Conclusion

In summary, we have proposed a poly-Si–based two-step TSV for the high temperature process of a VLS growth (> 700°C)–based Si-microneedle electrode array. The fabricated TSV shows the two step geometry, which inside is covered with a layer of heavily-doped poly-Si for the electrical connection. Current-voltage characteristics of the fabricated TSV show a linear behavior with the resistance of 6 kΩ. Although, additional processes of device metallization and encapsulation will be required for device completion, these results suggest the feasibility of the proposed TSV.

Acknowledgements

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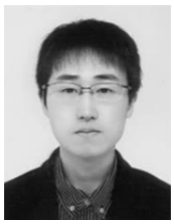

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