Supporting information

Metal interconnection process

The nanotip microwire array can be united with metal interconnections via integrated circuit processes prior to VLS growth of the silicon microwire. We began with a (111) silicon substrate (2 inch, p-type, resistivity=0.1 $\Omega \cdot$cm), consisting of n-type (resistivity of 10^{-3} $\Omega \cdot$cm) regions formed by selective phosphorous diffusion. The multiple layered metal system of WSi (300 nm)/TiN (50 nm)/Ti (50 nm) deposited by sputtering was used for the metal interconnection for subsequent VLS growth (500°C–700°C) (Fig. SI1a) [1]. The nanotip silicon microwire formed at the n-type region by the VLS growth and a sharpening technique (Fig. SI1b) [2]. Then a wire metal coating was realized by sputtering (Pt or Au, Fig. SI1c) and encapsulating the entire wire with an insulating layer (SiO$_2$ or parylene-C, Fig. SI1d). The entire wire was covered with a photoresist by spray coating (Fig. SI1e) the tip exposed by cycled photoresist etching. After exposing the nanotip section from the shell, the photoresist was removed to complete the device (Fig. SI1f–h).

Pt/Ti coated silicon nanotip

To confirm the conformal Pt coating over the silicon-nanotip section with ~40 degree angle, we employed transmission electron microscope (TEM) observations and energy dispersive x-ray spectroscopy (EDS) analysis. Figures SI2a and SI2b are the schematic and TEM images of the nanotip section of a microwire after Pt (30 nm)/Ti (20 nm) sputtering, respectively. The sputtering parameters for the Pt over the Ti/silicon nanotip were RF power of 50 W and a sputtering pressure of 0.5 Pa for 10 min. The curvature radius of the tip prior to the metallization was 50 nm, but increased to 70 nm after metallization (Fig. SI2b, c). A silicon nanotip with a 40 degree angle could be completely covered with Pt nanoparticles, as shown in TEM images (Fig. SI2b, c). Figure SI2d is the result of the EDS analysis. The only peak in

the Pt spectrum at 2.048 eV indicated that the wire nanotip was completely covered with Pt nanoparticles [3].

Electric field simulation by ANSYS

The dielectrophoretic (DEP) force is one scenario for nanoparticle trapping in a solution. As discussed in the main text (see formula (1) in the main text), the particle trapping force is proportional to ∇E^2. We calculated the electric field distributions in DIW while applying device biases to the Au-nanotip wire (simulated parameters: permittivity of DIW=80; and resistivity of DIW=10×10^6 $\Omega\cdot$ cm) by utilizing the finite element method analysis (ANSYS, Ansys Inc., Canonsburg, USA) [4]. Herein, the Au nanotip has a curvature radius and exposure height of 150 nm and 2 μm, respectively. The diameter of the microwire body is 2 μm, and the thickness of the parylene (permittivity = 3.15, resistivity = 8.8×10^{16} $\Omega\cdot$ cm) is 1 μm. The electrode model is consistent with the fabricated device (Fig. 2f in the main text). The calculated maximum electric field in this system occurs at the tip section of the wire. Figure SI4a shows the electric field distribution calculated with a threshold device bias of 20 mV, and the maximum electric field occurs at 6.19×10^3 V/m.

The effect of the nanotip formation on the electric field distribution was confirmed by calculating the electric field using a microwire with a 2 μm diameter hemispherical tip, which is consistent with the tip shape of the wire before the nanotip formation. Herein, the height of the exposed Au area has the same value (2 μm). To clarify the effect of nanotip formation on the electric field distribution, other parameters such as the diameter of the microwire body and the thickness of the parylene are same as the wire model used in the calculation of the Au nanotip. Figure SI4b shows the electric field distribution calculated with a device bias of 20 mV. The maximum electric field is 3.11×10^3 V/m, which is 1.99 times lower than that of the

nanotip, and is distributed around the hemispherical tip of the wire, but the nanotip wire yields a higher electric field with a small spot area for low bias and local trappings of particles.

Bias-induced particle holding force

We also demonstrated that an injection with the same device bias (1.0 V) was applied to both wire penetration and extraction, and fluorescence microscopy confirmed the particles were released to gelatin (Fig. SI5). These observations indicate that the applied holding force of 1.0 V is smaller than the adhesion force between the nanoparticle and gelatin ($F_{Par-Gel}$) and the device threshold voltage to hold the particles while penetrating the gelatin should be greater than the 1.0 V bias-induced holding force. As previously discussed, holding voltages greater than 2.0 V cannot be used in this scheme because electrolysis of the solution at the Au-nanotip section will occur. Although the applied 1.0 V–biased holding force is small, we did not use a device bias during wire extraction to eliminate the device bias–induced particle-holding force, resulting in only the forces of $F_{Par-Gel}$ and F_{Au-Par} in the particle release during the wire extraction. [Fig. SI7 and formula (4) in the main text].

SI references

[1] Takei, K., Kawashima, T., Kawano, T., Takao, H., Sawada, K., Ishida, M., 2008. Journal of Micromechanics and Microengineering 18(3), 035033.

[2] Goryu, A., Ikedo, A., Ishida, M., Kawano, T., 2010. Nanotechnology 21(12), 125302.

[3] McNab, J., Sandborg, A., The EDAX EDITOR, 14(1), 37.

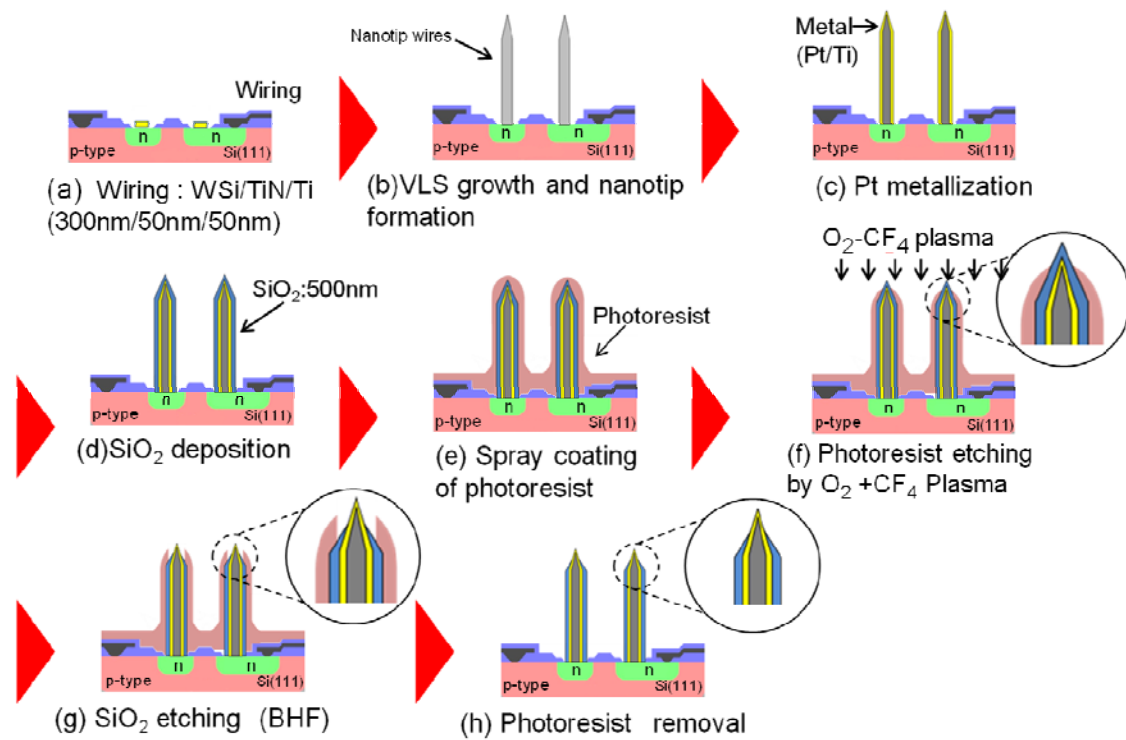[4] Mcintyre, C.C., Grill W.M., 2001. Annals of Biomedical Engineering 29(3), 227-235.

Figure SI1.

Process sequence to integrate nanotip electrode microwires with metal interconnections: a–b) IC processed interconnection followed by VLS growth of a Si microwire and the nanotip formation, c) wire metallization, d) SiO_2 deposition, e) spray coating of the photoresist, f) photoresist etching using O_2/CF_4 plasma, g) SiO_2 etching using BHF, and h) photoresist removal.
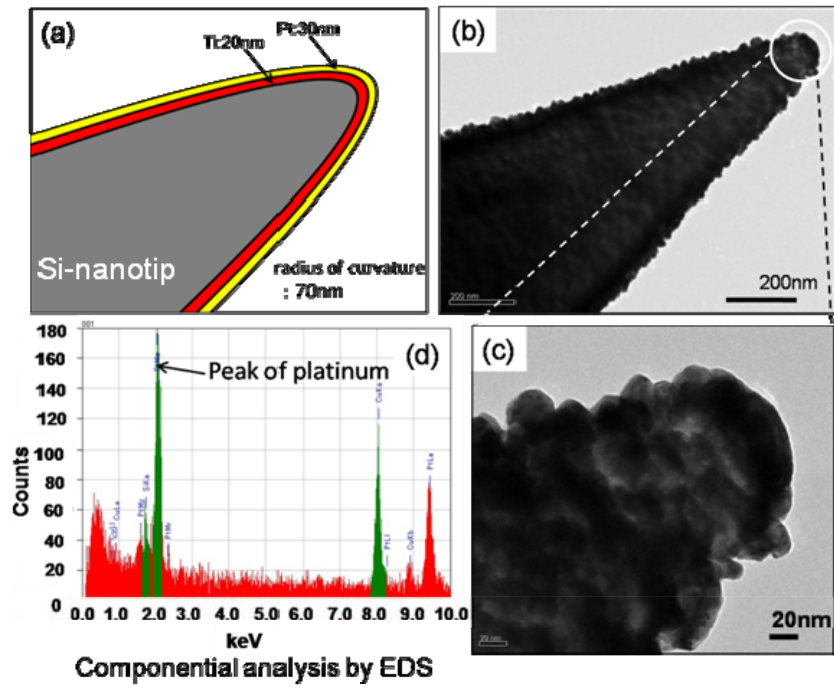
Figure SI2.

TEM images of a Pt/Ti/Si nanotip after metal deposition. a) Schematic diagram of the metalized nanotip wire. b–c) TEM images of the tip. d) Component analysis of the tip section by EDS.
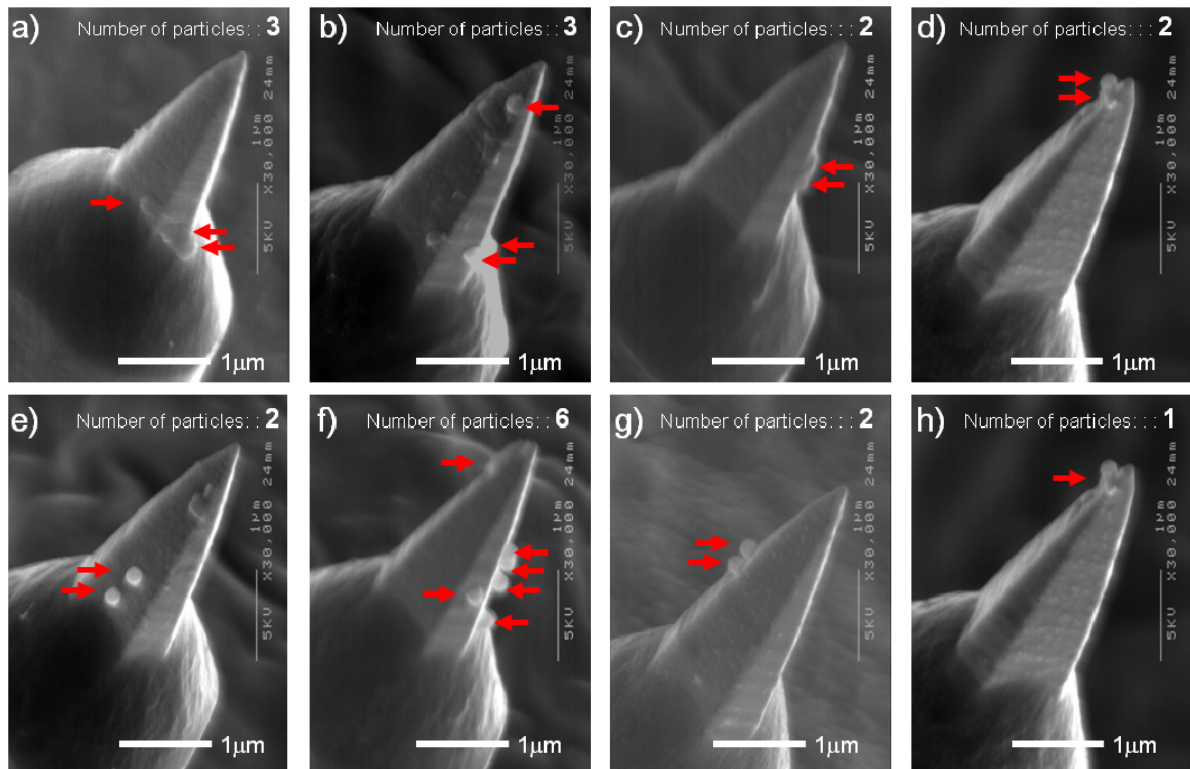
Figure SI3.

Nanoparticles trapped at nanotip wire samples in an array. Red arrows mark trapped nanoparticles. Particle trap has a device bias of 1.0 V. The maximum number of particles pre wire is 6, as shown in the image of (f). The average number of particles taken from 15 wire samples (these SEM images (a-h) are selected from observed 15 samples) is 2.1. These particle numbers represent observations on one side of the tip section.
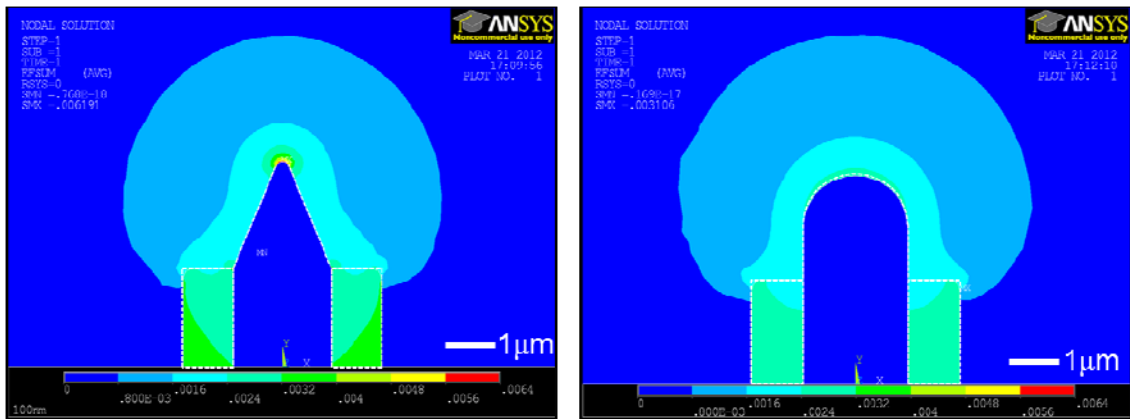
Figure SI4.

Calculated electric field distributions of (a) Au-nanotip wire with the curvature radius of 150 nm and (b) Au microwire with the 2 μm diameter hemispherical tip using the finite element method. Electric field at the nanotip section is approximately twice that at the hemispherical tip of the microwire.
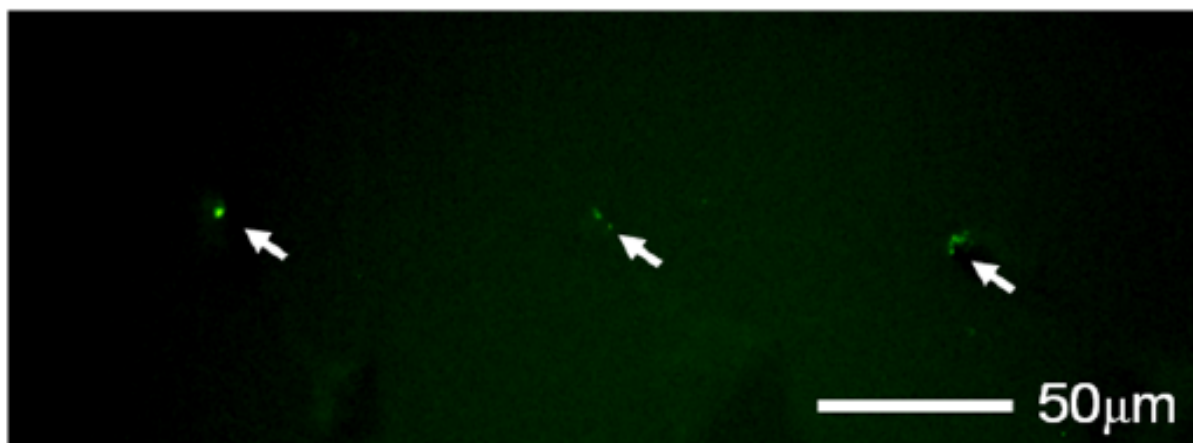
Figure SI5.

Top-view of the fluorescence image of a gelatin after nanoparticle injection. A constant device bias of 1.0 V was employed during the wire penetration and extraction. Nanoparticles transferred to the gelatin were observed at wire penetrated sites (Olympus BX51, Olympus, Japan).
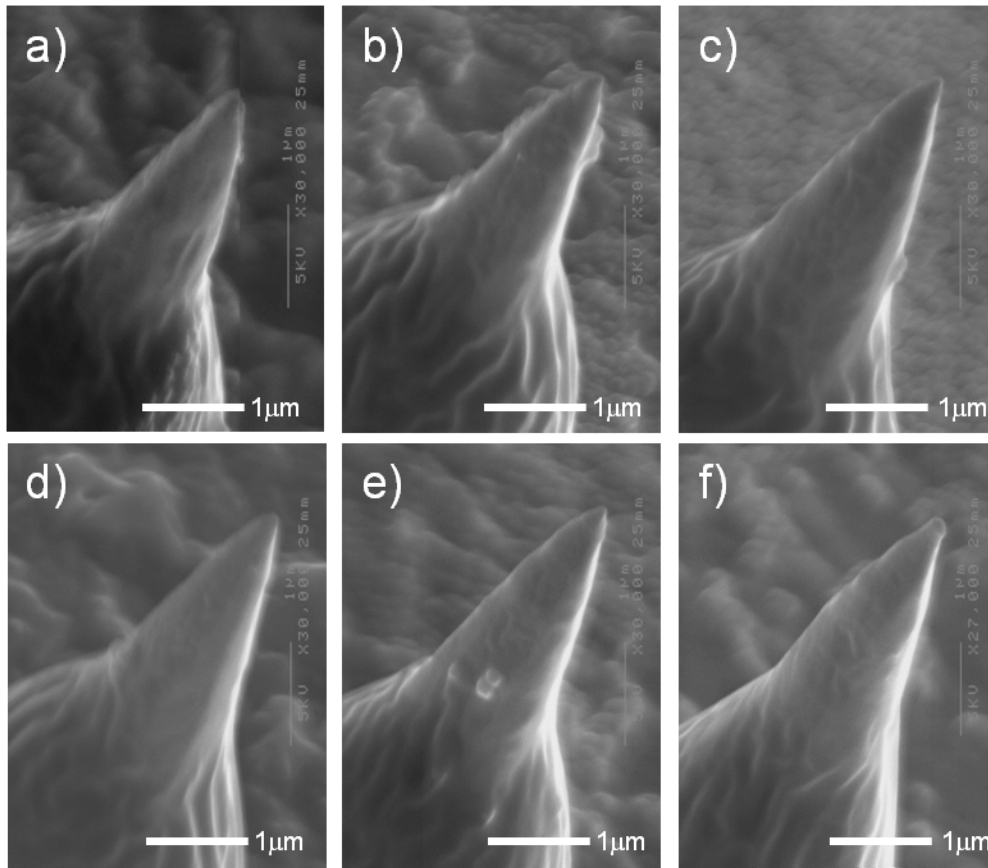
Figure SI6.

Nanotip wires in an array after one session of gelatin injection. No particles at nanotip are observed in the image of (a, c, d, and f), while other samples hold particles at its tips (b and e) after the wire penetration (device bias: 1 V) and extraction (0 V).
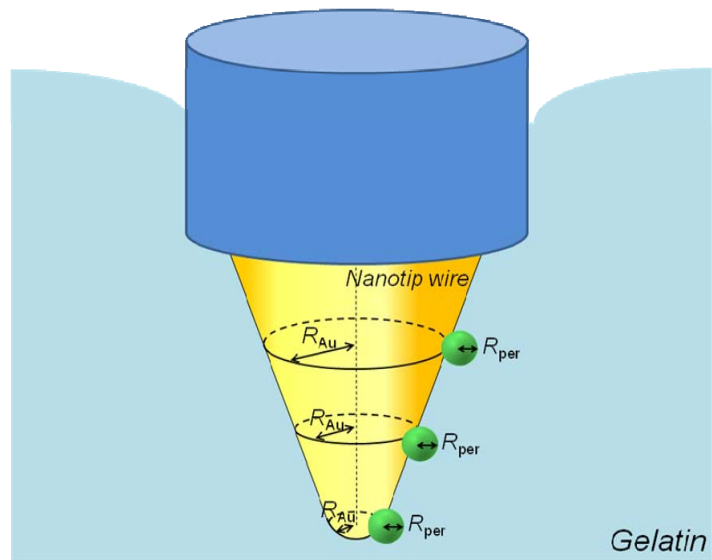
Figure SI7.

Schematic image used to model the adhesion forces between a nanoparticle and the Au-nanotip wire and between the nanoparticle and gelatin. R_{Par} is the radius of a nanoparticle and R_{Au} is the curvature radius of the area in the Au electrode where the nanoparticle is trapped.