Appendix A: The equivalent circuit model

Parasitic capacitances

The equivalent circuit model of the Si microprobe array chip is depicted in Figs. 3a and 3b. The impedance Z_{para1} consists of parasitic capacitances existing at the probe side (C_{side}) and between the metal and saline ($C_{metal/saline}$). C_{side} was applied to the coaxial model.

$$C_{side} = \frac{2\pi\varepsilon_0\varepsilon_{INS}h_P}{\ln\frac{r_P}{r_P - d_P}} \quad \text{(A.1)}$$

$C_{metal/saline}$ was considered as a parallel plate type capacitance model.

$$C_{metal/saline} = \frac{S_M}{\frac{d_{INS}}{\varepsilon_0\varepsilon_{INS}} + \frac{d_{BR}}{\varepsilon_0\varepsilon_{BR}}} \quad \text{(A.2)}$$

where ε_0 is the dielectric permittivity of free space; ε_{INS} is the relative dielectric constant of SiO_2 insulating layer; h_P is the probe height; r_P and d_P are the probe radius and thickness of insulating layer, respectively; S_M is the horizontal area of the metal interconnection; d_{INS} and d_{BR} are thicknesses of the top insulating layer and the black resist light-shielding layer, respectively; and ε_{BR} is the relative dielectric constant of black resist.

Other parasitic capacitances exist at the p-n junction ($C_{p\text{-}n}$), between the metal interconnection and the substrate ($C_{metal/substrate}$), and between signal lines and a reference line of the bundled cable (C_{cable}). The parasitic impedance Z_{para2} was consisted with these three capacitances ($C_{p\text{-}n}$, $C_{metal/substrate}$, C_{cable}). First, the p-n junction of the Si microprobe array chip is a one-side abrupt type (Sze, 2001),

because of the quite high-doping concentration of the n-type region. The depletion layer capacitance ($C_{p\text{-}n}$) is calculated from the built-in potential,

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^{\,2}} \right), \tag{A.3}$$

and the depletion-layer width,

$$W \cong \sqrt{\frac{2\varepsilon_s \varepsilon_0 (V_{bi} - V)}{qN_D}}, \tag{A.4}$$

as

$$C_{p-n} = A_{p-n} \frac{\varepsilon_s \varepsilon_0}{W}, \tag{A.5}$$

where k is the Boltzmann constant; T is the absolute temperature; q is the elementary charge; N_D and N_A are donor- and accepter-impurity densities, respectively; n_i is the intrinsic carrier concentration; W is the depletion-layer width; ε_s is the relative dielectric constant of Si; V_{bi} is the built-in potential, which is electrostatic potential difference between the p-side and the n-side neutral regions at thermal equilibrium; V is the bias potential (here, we use input voltage during test signal recording); and $A_{p\text{-}n}$ is the area of depletion-layer. Second, the parasitic capacitance between the metal interconnection and the substrate ($C_{metal/substrate}$) is calculated by

$$C_{metal\,/\,substrate} = \frac{\varepsilon_0 \varepsilon_{INS} S_W}{d_{SUB}}, \tag{A.6}$$

where S_M is the area of the metal interconnection on the p-well substrate; and d_{SUB} is the thickness of SiO_2 layer between the interconnection and the Si substrate. Third, the parasitic capacitance between signal lines and a reference line of the bundled cable (C_{cable}) is measured by a capacitance meter

(DT-117; HOZAN, Japan).

The details of the numerical values are described as following. Three of capacitances C_{side}, $C_{metal/saline}$, and $C_{metal/substrate}$ are calculated by designed values: h_P = 40 μm, r_P = 1.75 μm, d_P = 500 nm, d_{INS} = 1.35 μm, d_{BR} = 1 μm, d_{SUB} = 1.8 μm, S_M = 3.5 mm×10 μm, and S_W = 0.6 mm×10 μm. $C_{p\text{-}n}$ is calculated by values: V_{bi} = 0.9 V (N_A= 10^{16} cm^{-3}, N_D = 10^{19} cm^{-3}, n_i = 9.65×10^9 cm^{-3}, T=300 K), $W|_{V\,=\,\pm 80\ \mu m}$ = 1.01 μm, and $A_{p\text{-}n}$ = 10 μm×10 μm. As results, C_{side} = 0.03 pF, $C_{metal/saline}$ = 0.46 pF, $C_{p\text{-}n}|_{V=\pm 80 \mu V}$ = 0.9 pF, and $C_{metal/substrate}$ = 0.1 pF were obtained by Eq. (A.1) - (A.5) (where ε_{INS} = 3.8, ε_{BR} = 3.2, ε_s = 11.9). In addition, C_{cable} became 130 pF.

Resistance

The resistance of each metal interconnection [300-nm-thick tungsten silicide (WSi_2) / 50-nm-thick titanium nitride (TiN) / 50-nm-thick titanium (Ti)] of the Si microprobe chip is given by

$$R_{wire} = R_s \cdot \frac{L_{wire}}{W_{wire}}, \qquad \text{(A.7)}$$

where R_{wire} is the resistance of metal interconnection; R_S is the sheet resistance of the interconnection (3.43 Ω·cm); L_{wire} and W_{wire} are the length and width of the interconnection, respectively (L_{wire} = 3.5 mm, W_{wire} = 10 μm). The calculated resistance R_{wire} was 1.2 kΩ, which is largest resistance value in the used recording system [from the Si microprobe chip section to the pre-amplifier section, see Fig. 3 (b)].

Appendix B: Crosstalk capacitances

Crosstalk caused by parasitic coupling capacitance between adjacent interconnections becomes a serious problem in MEA design. Crosstalk is a noise and causes interferences and delay faults. Figure B shows two-line interconnections and their coupling capacitance (C_m). If one line (A) starts a falling transition while the other line (B) is having a rising transition, the waveform on line B may be distorted and the delay will be increased. While line A is active, the current going through the coupling capacitance is $C_m(\Delta V_A - \Delta V_B) / \Delta t$. If two lines are simultaneously active in the same direction, the signal interference and delay will not occur because the current does not flow through the coupling capacitance.

In this study, total crosstalk capacitance between adjacent interconnections [integrated interconnections of the Si microprobe chip (C_{metal} = 0.8 pF), interconnections from the ceramic package section to the circuit board section (C_{pack} = 3 pF, measured value), and signal lines of the bundled cables from the circuit board to the pre-amplifier section (C_{line} = 30 pF, measured value)] is 33.8 pF. If neural signal flows through the one line alone and neighbor line is quite, the O/I ratio associated with the crosstalk capacitance decreases from 57% to 54% at 200 Hz. The crosstalk has little influence on ERG recordings. When the uniform light stimuli to the entire retina were used and the evoked retinal signals were simultaneously inputted to all recording channels via Si microprobes, the crosstalk capacitance between adjacent interconnections can be neglected because no current

flows through the coupling capacitances.

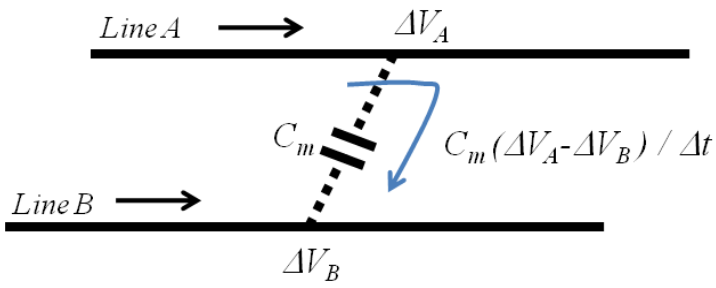

Fig. B Coupling capacitance

Reference

Sze, S. M., Semiconductor Devices: Physics and Technology, 2nd Edition, 2001. Wiley

Appendix C: Inverse filter for the compensation function, H_N^{-1}

We used a curve fitting technique to obtain the compensation function (H_N^{-1}) (Fig. 4c). Because both the amplitude and phase of the transfer function (H_N) of the neural recordings exhibit the characteristics with a low-pass behavior, these characteristics can be expressed as sigmoid curves in the frequency domain ($f = \omega/2\pi$). The inverse filter (H_N^{-1}) can be obtained based on the amplitude and the phase. The equation of the sigmoid function is as follows:

$$H_N(f) = \frac{L}{1 + \alpha \exp\{\beta[\log_{10}(f) + \gamma]\}} \qquad \text{(C.1)}$$

where L is the maximum H_N; α is the parameter to shift the inflection point toward the axis direction of the frequency; β is the amount of change in H_N; f is frequency; and $\log_{10}(f)$ for logarithmic

behaviors (Mathews, 1992). In this paper, we added the correction term, γ, to the equation, in order to reduce approximation errors. The compensation curve for the amplitude, G_{amp} (= H_N^{-1}), is the inverse of the sigmoid function as shown in Eq. (9). The compensation curve for the phase, θ_c (= –arg H_N), is the opposite of the sigmoid function as shown in Eq.10. H_N^{-1} is a complex signal with G_{amp} and θ_c as shown in Eq. (8). The following list shows the relationship between the model parameters and compensation curves.

α: If this value increases, the characteristic curve (G_{amp}) is shifted to the low-frequency side.

β: If this value increases, the amount of change in G_{amp} increases.

γ: If this value increases, the amount of change in G_{amp} increases slightly.

η: If this value increases, the characteristic curve (θ_c) is shifted to the high-frequency side.

λ: If the absolute of this value increases, the amount of change in θ_c increases.

τ: If the absolute of this value increase, the characteristic curve (θ_c) is shifted slightly to the high-frequency side.

Reference:

John H. Mathews, Numerical methods for mathematics, science, and engineering 2nd edition, Prentice-Hall, Inc., 1992: Chapter 5 Curve Fitting, pp. 257 – 314.

Appendix D: The systematic analysis using the parasitic impedance model

Our systematic analysis using the parasitic impedance model allows optimal configurations of both the Si microprobe chip and the recording system. In order to obtain an O/I ratio of more than 90% ($|Z_{load}|$ = 80 MΩ; $|Z_{para1}|$ = 325 MΩ; $|Z_{para2}|$ = 1.2 MΩ, at 1 kHz), the required probe impedances can be expected to be less than 500 kΩ at 200 Hz for ERG recordings (frequency ~500Hz in typical ERG recordings) and less than 120 kΩ at 1 kHz for spike recordings (~10 kHz in typical spike recordings) [Fig. D(a)]. However, to achieve these impedances, an Au probe tip with a diameter of more than 20 μm would be required, which would negate the low-invasiveness of the probe penetration. To reduce the probe impedance without increasing the probe-tip diameter, a material with low-impedance characteristics in saline [e.g., platinum (Pt) black or iridium oxide (IrO_x)] can be used as the tip material for the Si microprobe (Oka et al., 1999; Mailley et al., 2002).

On the other hand, we have currently developed a silicon microprobe with a tip diameter of ~50 nm (Goryu et al., 2010). The nanotip probe provides intracellular recordings with large neural amplitudes (~100 mV). Though we expect the high impedance of the nanoprobe associatedwith decreasing the recording area, the impedance of the nanoprobe canbe reduced by utilizing aforementioned materials (Pt, IrO_x). Once neural responses are obtained via the nanoprobes, we can use the signal compensation method. The results of a small diameter high density nanoprobe array-based multi-site intracellular recording of the retina are forthcoming.

Our systematic analysis also determined that the parasitic capacitance configuration for the recording system [p-n junctions ($C_{p\text{-}n}$) and metal interconnections ($C_{metal/substrate}$) in the chip device and outer cables (C_{cable})] should be minimized. The parasitic impedance $|Z_{para2}|$, consisting of a parasitic resistance (R_{para}) and parasitic capacitances ($C_{para2} = C_{p\text{-}n} + C_{metal/substrate} + C_{cable}$), was 1.2 MΩ at 1 kHz, a value similar to the probe impedance (1.3 MΩ at 1 kHz). Consequently, the recorded 48% signal amplitude was mainly reduced by this parasitic impedance. Based on the parasitic impedance value, higher O/I ratios, more than 80% at 1 kHz, would be possible with reduced parasitic capacitances (C_{para2}) of less than 10% (13.1 pF) [Fig. D(b)]. The reduction of these parasitic capacitances also helps to reduce crosstalk associated with adjacent interconnections. To reduce the effects of signal attenuation, phase delay, and crosstalk, (i) expanding the interconnection spacing, (ii) shortening the length of interconnections between the chip and the pre-amplifier, and (iii) integration of on-chip pre-amplifier circuitry (Sodagar et al., 2007) should be addressed in future studies.

References:

Oka, H, Shimono, K., Ogawa, R., Sugihara, H., Taketani, M., 1999. Journal of Neuroscience Methods 92, 61-67.

Mailley, S. C., Hyland, M., Mailley, P., McLaughlin, J. M., McAdams, E. T., 2002. Materials Science

and Engineering 21, 167-175.

Goryu, A., Ikedo, A., Ishida, M., Kawano, T., 2010. Nanotechnology 21(12), 125302.

Sodagar, A. M., Wise, K. D., Najafi, K., 2007. IEEE Trans. Biomed. Eng. 54, 1075-1088.

(a) (b)

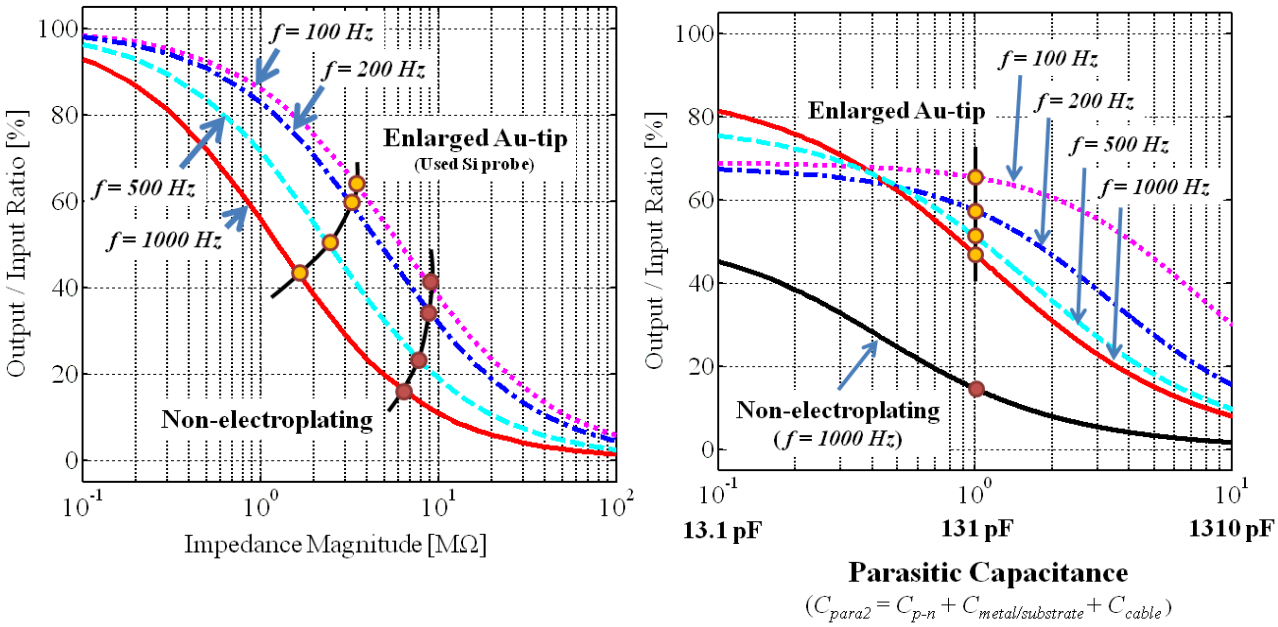

Fig. D The systematic analysis using the parasitic impedance model brings optimum configurations of the Si probe chip and the recording system. (a) Estimated O/I ratio versus probe impedance. The O/I ratio decreased with the enlarged Au-tip (yellow circles: enlarged Au-tipped Si microprobe, red circles: non-electroplated Si microprobe). The O/I ratio of the non-electroplated Si microprobe was estimated by using the measured impedance of the Si probe chip section and the recording system (the cable and load impedances). (b) The estimated O/I ratio versus parasitic capacitance value (C_{p2} = $C_{p\text{-}n}$ + $C_{metal/substrate}$ + C_{cable}.).