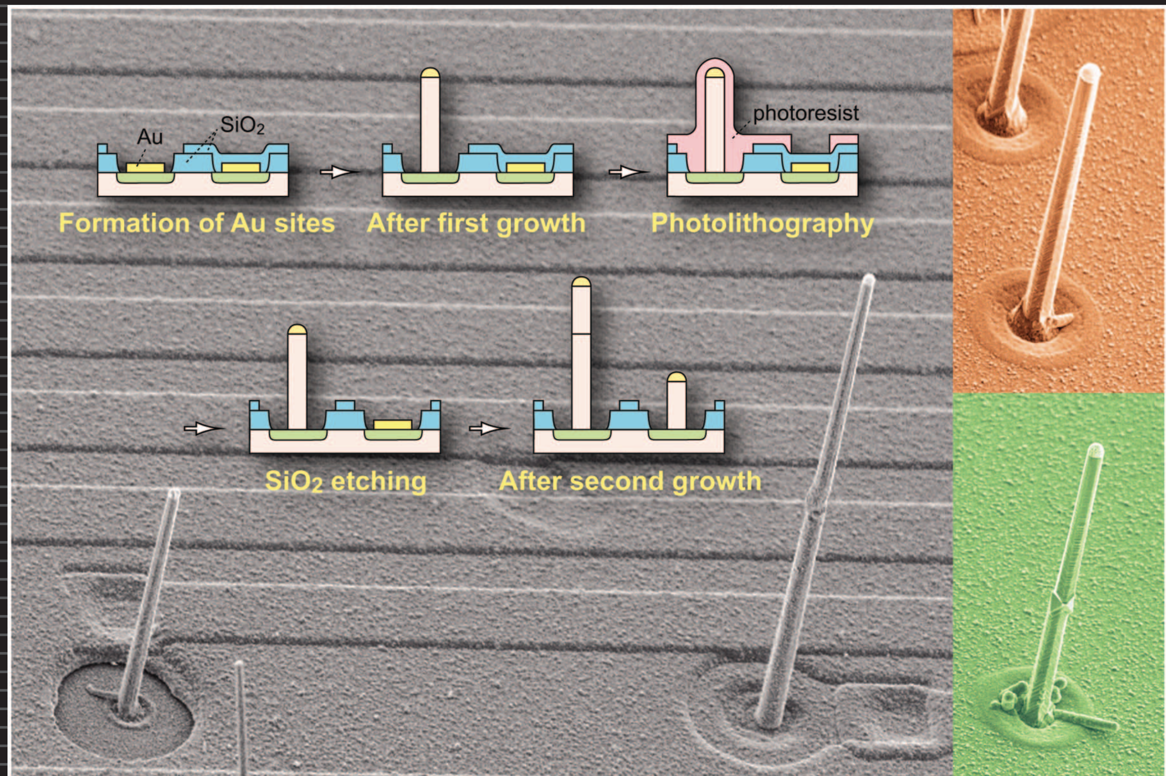
Articles published week of 20 JULY 2009
Volume 95 Number 3

APPLIED PHYSICS LETTERS



0003-6951(20090720)95:3;1-M

AMERICAN INSTITUTE OF PHYSICS

Vertically aligned silicon microwire arrays of various lengths by repeated selective vapor-liquid-solid growth of *n*-type silicon/*n*-type silicon

Akihito Ikedo,[1,a)] Takahiro Kawashima,[2] Takeshi Kawano,[1] and Makoto Ishida[1]
[1]*Department of Electrical and Electronic Engineering, Toyohashi University of Technology, Toyohashi, Aichi 441-8580, Japan*
[2]*Department of Production System Engineering, Toyohashi University of Technology, Toyohashi, Aichi 441-8580, Japan*

(Received 29 December 2008; accepted 13 May 2009; published online 21 July 2009)

Repeated vapor-liquid-solid (VLS) growth with Au and PH_3–Si_2H_6 mixture gas as the growth catalyst and silicon source, respectively, was used to construct *n*-type silicon/*n*-type silicon wire arrays of various lengths. Silicon wires of various lengths within an array could be grown by employing second growth over the first VLS grown wire. Additionally, the junction at the interface between the first and the second wires were examined. Current-voltage measurements of the wires exhibited linear behavior with a resistance of 850 Ω, confirming nonelectrical barriers at the junction, while bending tests indicated that the mechanical properties of the wire did not change. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3178556]

The vapor-liquid-solid (VLS) growth method[1] is commonly used to synthesize one-dimensional semiconducting nanowires, carbon nanotubes, and microwires for various applications, including optical,[2] biochemical sensors,[3] and nanoelectromechanical system/microelectromechanical system (NEMS/MEMS) devices.[4,5] To achieve the device fabrication, it is necessary to control the size (diameter) and position of the wire. Fortunately, these can be achieved by lithographic patterning of the catalytic particles and subsequent VLS growth.[6–8] In addition, a constant growth rate which depends on the growth temperature and pressure of the gas source, can control the wire length. We have demonstrated VLS growth of a silicon microwire array, which had a controlled diameter and length of ~3 and ~300 μm, respectively, and applied this method to insert a microwire array into neuronal tissue in order to detect neural signals.[9]

VLS growth yields wire arrays with similar wire lengths when the same growth conditions (e.g., temperature, pressure, and time) are used. Typical conditions used to grow 30 μm wire arrays resulted in wire lengths from 29.1 to 31.7 μm. The scale of these variations is acceptable for our application. Although VLS growth provides sub- to several-micron variations in wire length, individually controlling the ten/hundred micron-scale length of a wire in the same array remains problematic. To realize wires with different lengths, herein we demonstrate repeated selective VLS growth of silicon microwires using a catalyst, which remains at the tip of the first wire grown. In the first VLS growth step, several wires are grown from catalytic-Au particles, while the other particles in the array are covered with a silicon dioxide (SiO_2) layer to prevent from a reaction during the first VLS growth. After exposing the particles underneath the SiO_2 layer, a second VLS growth is carried out to grow wires from both the particles at the tips of the first wires (for longer wires) and particles at the substrate (for shorter wires), resulting in an array composed of different length wires. In fact, the longer wires show a change in wire diameter in the middle portion of the wire body, indicating an interface junction between the bottom of the second wire body and the tip of the first wire body. In addition, the electrical and mechanical characterizations of the junction are discussed.

Figure 1 schematically illustrates the process of repeated selective VLS growth to realize an array with *n*-type silicon microwires of different lengths. Selective VLS growth can be carried out after integrated circuit processes.[9–11] We began with a silicon (111) substrate (*p*-type with a resistivity of 0.1 Ω cm). The heavily doped *n*-type region (resistivity of 10^{-3} Ω cm) was formed by selective phosphorus diffusion where a silicon wire could be located in the VLS growth. Each wire region was connected with individual interconnec-

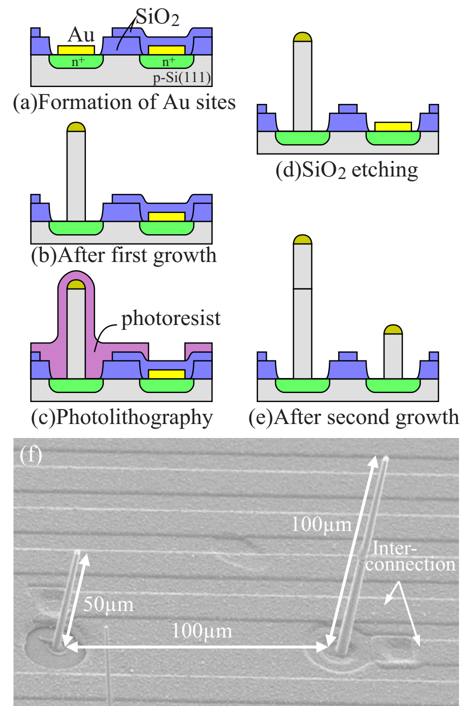


FIG. 1. (Color online) [(a)–(e)] Process flow for simultaneous integration of two vertically aligned, different length silicon microwires by repeated selective VLS growth. (f) SEM image of a 100 μm silicon wire and a 50 μm silicon wire integrated with on-chip metal interconnections.

[a)]Electronic mail: ikedo-a@dev.eee.tut.ac.jp.

 © 2009 American Institute of Physics

Downloaded 22 Jul 2009 to 133.15.22.66. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

tions of 400-nm-thick WSi/TiN/Ti for electrical measurement applications.[11] A 160-nm-thick Au film was formed by evaporation, and was patterned by lift-off, resulting in a 4 μm Au particles array. To grow silicon wires in the first VLS growth, a gas source of silicon was employed, while the other Au catalysts, which were used in subsequent second VLS growth, were selectively covered with a 1 μm SiO_2 layer formed by plasma-enhanced chemical vapor deposition. After the first VLS growth, the particles underneath the SiO_2 layer were exposed by photolithography and chemical etching of SiO_2 by buffered hydrofluoric acid, and then the second VLS growth was performed to grow silicon wires from both the tip of the first silicon wire and the silicon substrate. A technique to spray coat a photoresist was used in the photolithography to completely cover silicon wires with a uniformly thick photoresist >2 μm, but the photoresist could be exposed using projection printing. Figure 1(f) shows the scanning electron microscope (SEM) image of a 100 μm wire and a 50 μm wire grown by repeated VLS growth (first and second VLS growths) and single step VLS growth (only second VLS growth), respectively. Herein a mixture gas of 1% PH_3 (diluted in 99% hydrogen) with 100% Si_2H_6 was used as the silicon gas source to obtain n-type silicon wires with a resistivity on the order of 10^{-2} Ω cm (impurity concentration is 10^{18} cm^{-3}).[12] All of VLS growths were performed at a gas pressure of 0.6 Pa and a growth temperature of 680 °C, which resulted in a growth rate of 1 μm/min and a higher yield of vertically aligned individual microwires. Using these VLS growth parameters, a polycrystalline silicon layer (<1 μm thick) was deposited over the SiO_2 layer, which could be removed with XeF_2 gas etching while the microwire was covered with a spray-coated photoresist.

Figure 2(a) shows the current I-voltage V characteristics of a single n-type/n-type silicon wire grown by repeated VLS growth at a PH_3 and Si_2H_6 ratio of 8000 ppm. Figure 2(b) shows the SEM image of the measured silicon wire. The I-V curves were acquired using two 5 μm tip diameter tungsten needles where one was in contact with the tip of the silicon wire, while the other was in contact with the base of the silicon wire. Due to lateral growth of silicon during VLS growth, the measured wire exhibited a circular-cone shape with a tip diameter of 2.2 μm, a bottom diameter of 3.1 μm, and a total wire length of 50 μm. The I-V curve displayed an electrical linear behavior under a voltage of ±1.0 V with an overall resistance of 850 Ω, which is similar to the behavior of a one-step wire with the same dimensions: 50 μm long, and tip and bottom diameter of 2.8 and 3.8 μm, respectively [Fig. 2(c)]. The measured one-step wire had a resistance of 890 Ω.

Actually, the interface junction might serve as an electrical discontinuous/barrier region in the wire. For example, changing the impurity concentration of phosphorus at the interface causes the electrical resistance in the wire body to change. In addition, we prepared a wire grown in two steps (tip diameter=3.0 μm, bottom diameter=3.8 μm, and length=40 μm), which also consisted of a similar laterally grown silicon region around the core silicon. The laterally grown region of the wire was etched by a plasma etching utilizing CF_4 gas, which resulted in only the core silicon wire body (tip diameter=1.6 μm, bottom diameter=2.4 μm, and length=40 μm). The I-V curve of the core silicon wire also exhibited a linear behavior, suggesting that a significant electrical barrier is not present at the interface of the core silicon wire body. The measured resistance of the core silicon wire was 843 Ω. Thus, the electrical resistivity of the wire ρ can be calculated using the resistance of the measured wire R and the volume of the wire (circular-cone shape: tip diameter a, bottom diameter b, and length l) as

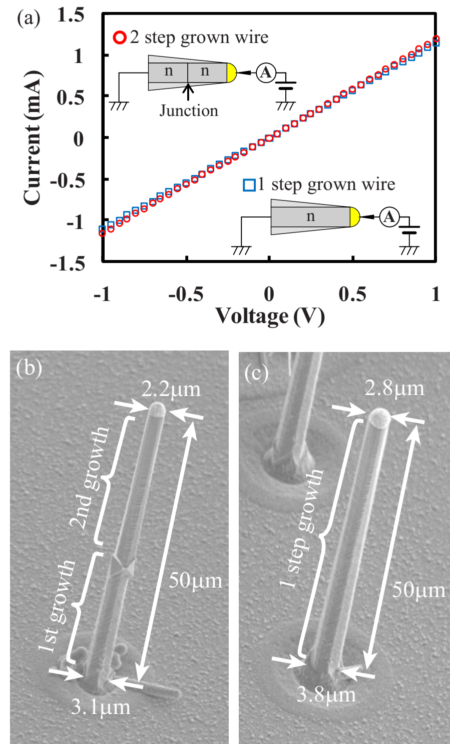


FIG. 2. (Color online) Electrical properties of the silicon microwire. (a) Current I-voltage V characteristics of n-type silicon/n-type silicon wire grown in two steps compared to n-type silicon wire grown in a single-step growth. I-V curves are taken between the tip and the bottom of the silicon wire using tungsten microdiameter needles. (b) SEM image of the measured wire grown in two steps with a junction in the middle portion of the wire body and (c) wire grown in one step without a junction.

$$\rho = \frac{\pi ab}{4l} R. \tag{1}$$

The formula yields a resistivity of 6×10^{-3} Ω cm (impurity concentration of 7×10^{18} cm^{-3}). Based on the comparison of I-V curves between VLS wires grown in one step and two steps shown in Fig. 2(a) and an additional measurement on a two-step grown core silicon wire, significant changes in the electrical properties of the wire body did not occur in the two-step VLS grown silicon wire consisting of a n-type/n-type system.

We expected that the mechanical properties of the two-step grown silicon wire would be the same as that of a one-step VLS grown silicon wire because the entire wire body must have a single-crystalline silicon structure, even though the wire consists of a junction area in the body. Figure 3(a) schematically shows an image of the bending test on a single silicon wire grown in two steps using a 5 μm tip diameter tungsten needle. Figure 3(b) shows the SEM of the tested typical silicon wire, which had a diameter of 3 μm and the total length of 25 μm (8 μm by the first growth and 17 μm by the second growth). Moreover, we predicted that the maximum stress associated with the bending force applied at the wire tip must be close to the base of the wire body. A

Downloaded 22 Jul 2009 to 133.15.22.66. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

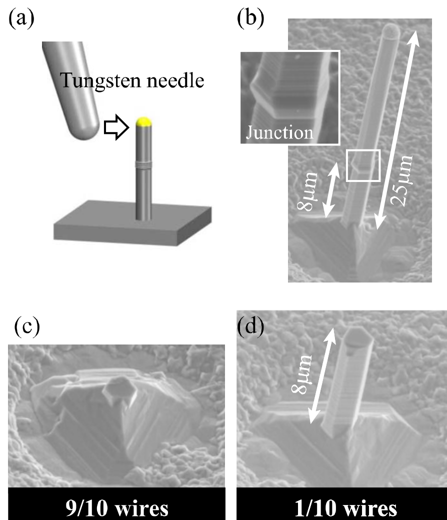


FIG. 3. (Color online) (a) Schematic of the bending test for a silicon microwire grown in two steps with a junction. (b) SEM image of the tested wire. Inset image shows the junction site located 8 μm above the base. (c) Typical SEM image of a broken wire at the base (nine of ten wires in the test) and (d) broken at the junction site (one of ten wires in the test).

bending force via the tungsten needle was applied at the wire tip until the wire broke. Consequently, nine of the ten wires broke at the base of the wire [Fig. 3(c)]. Only one wire in the test indicated that the breakdown portion was at the junction site located 8 μm above the substrate, as shown in Fig. 3(d). This breakdown behavior is probably due to the nick shape at the junction, which was formed by the change in the diameter of the catalyst at the beginning of the second VLS growth.

In summary, various lengths of silicon wires were fabricated in the same array by selective repeated VLS growth. Although a junction is found at the interface between the wire bodies, significant changes do not occur in the electrical and mechanical properties of the wire. Based on the capability of the repeated growth of silicon wire, a large number of wires of various lengths for electrical recording of neurons should be possible. This technique may also enable vertically aligned microwires with p-n junctions for electrical/optical device applications, using p-type[13] and n-type gas sources (e.g., PH_3- and B_2H_6–Si_2H_6 mixtures). Although herein we only demonstrate vertically aligned silicon wire of various lengths for microscale device fabrications, this technique should be applicable to nanoscale device fabrications.

The authors would like to thank Kuniharu Takei for the fruitful discussion and Mitsuaki Ashiki for his assistance with the fabrication processes. This work was supported by a Grant-in-Aid for Scientific Research (S), by the Global COE Program "Frontiers of Intelligent Sensing" and by Strategic Research Program for Brain Sciences (SRPBS) from the Ministry of Education, Culture, Sports, Science and Technology of Japan (MEXT).

[1]R. S. Wagner and W. C. Ellis, Appl. Phys. Lett. **4**, 89 (1964).
[2]B. M. Kayes, H. A. Atwater, and N. S. Lewis, J. Appl. Phys. **97**, 114302 (2005).
[3]Z. Li, Y. Chen, X. Li, T. I. Kamins, K. Nauka, and R. S. Williams, Nano Lett. **4**, 245 (2004).
[4]A. M. Fennimore, T. D. Yuzvinsky, W.-Q. Han, M. S. Fuhrer, J. Cumings, and A. Zettl, Nature (London) **424**, 408 (2003).
[5]A. S. Paulo, N. Arellano, J. A. Plaza, R. He, C. Carraro, R. Maboudian, R. T. Howe, J. Bokor, and P. Yang, Nano Lett. **7**, 1100 (2007).
[6]B. M. Kayes, M. A. Filler, M. C. Putnam, M. D. Kelzenberg, N. S. Lewis, and H. A. Atwater, Appl. Phys. Lett. **91**, 103110 (2007).
[7]T. Sato, K. Hiruma, M. Shirai, K. Tominaga, K. Haraguchi, T. Katsuyama, and T. Shimada, Appl. Phys. Lett. **66**, 159 (1995).
[8]Y. Okajima, S. Asai, Y. Terui, R. Terasaki, and H. Murata, J. Cryst. Growth **141**, 357 (1994).
[9]T. Kawano, Y. Kato, M. Futagawa, H. Takao, K. Sawada, and M. Ishida, Sens. Actuators, A **97**, 709 (2002).
[10]T. Kawano, Y. Kato, R. Tani, H. Takao, K. Sawada, and M. Ishida, IEEE Trans. Electron Devices **51**, 415 (2004).
[11]K. Takei, T. Kawashima, T. Kawano, H. Takao, K. Sawada, and M. Ishida, J. Micromech. Microeng. **18**, 035033 (2008).
[12]M. S. Islam, H. Ishino, T. Kawano, H. Takao, K. Sawada, and M. Ishida, Jpn. J. Appl. Phys., Part 1 **44**, 2161 (2005).
[13]M. S. Islam, T. Kawashima, K. Sawada, and M. Ishida, J. Cryst. Growth **306**, 276 (2007).

Downloaded 22 Jul 2009 to 133.15.22.66. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp