Paper

Signal Conditioning CMOS Circuits Integrated on Si (111) for Image-Recording Sensor of Neural Activity

Yoshiko Kato*, Member, Takeshi Kawano*, Member
Yoshiaki Ito*, Non-member, Hidekuni Takao*, Member
Kazuaki Sawada*, Member, Makoto Ishida*, Member

An on-chip signal conditioning CMOS Integrated Circuit on Si (111) was fabricated for use in multi-point neural activity recording. The two-dimensional (2D) micro-Si probe array for neural activity recording sensor can be fabricated on the IC by Vapor-Liquid-Solid (VLS) growth method. However, the circuit has to be fabricated on Si (111) wafer because micro-Si probe is grown perpendicularly only on Si (111) wafer. Proper process conditions were established for fabrication of CMOS on Si (111). The circuits include 8×8 array of signal conditioning pixels with two 8-bit shift registers as 2D scanning circuits and a frequency divider. It is found from evaluated results of the fabricated circuits on Si (111) that CMOS circuits can be formed on Si (111) with enough performance. The output signal is detected from the selected pixel with the circuit. Increasing the potential at the selected pixel, the output signal increases in proportion to the potential. It has been confirmed that circuits on Si (111) are possible to be realized and available for image-recording sensor of neural activity.

Keywords : CMOS on Si (111), image recording, smart neural sensor, micro-Si probe array, vapor-liquid-solid growth

1. Introduction

In in-vivo studies, multipoint recordable Si probe arrays of penetrating needle type with same size as the neurons allow researchers to reconsider the neuron system [(1)~(4)]. We have proposed a smart image-recording sensor of neural activity with signal processing circuits and micro-Si probe array integrated on the same Si chip [(5)]. Figure 1 shows concept diagram of the image-recording sensor of neural activity with circuits and micro-Si probe array. This sensor is fabricated with CMOS technology and a selective Au-Si_2H_6 Vapor–Liquid– Solid (VLS) growth method. The VLS growth of single crystal Si probe is carried out on Si (111) wafer using Au dots formed with lift-off process and then Si_2H_6 gas source MBE [(6)]. Si probes can be grown perpendicularly and selectively in a few tens of micron intervals same as the neuron size by using selective VLS growth method. Those probes are suitable to measure the neurons, because the probes can be penetrated exactly and perpendicularly the neurons which are measuring objects. We have studied the Si probe array growth technology with on-chip n-MOSFET switching circuits on Si (111). As a result, n-MOSFET properties such as leakage current and threshold voltage were not affected significantly by VLS growth [(5)], and degradation of n-MOSFET due to Au diffusion during VLS growth is not serious.

Nevertheless, there are two problems that circuits have to be fabricated on Si (111) wafer with VLS growth. One of the problems is device performance degradation caused by existence of a large number of interface state density on Si (111) as compared with Si (100). Another problem in the fabrication process is high-temperature (500 °C ~ 700 °C) damage in the VLS growth process followed by CMOS process. In order to realize the image-recording sensor of neural activity, it is necessary to fabricate CMOS circuit on Si (111). In this study, CMOS Integrated Circuit for the image-recoding of neural activity was designed, fabricated, and evaluated. The fabricated circuit was designed for scanning two-dimensional (2D) signal distribution with enough operation speed for measurement of the neural activity signal. In this paper, the performances of CMOS Integrated Circuit on Si (111) for the image-recording sensor of neural activity are discussed.

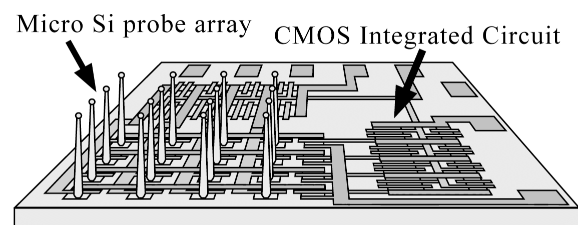


Fig. 1. Concept diagram of the image-recording sensor of neural activity with circuits and micro-Si probe array.

2. Configuration of Si (111) CMOS Circuit

Figure 2 shows the configuration of the image-recording circuit. The circuit, which is fabricated by CMOS technology, is able to scan 2D signal distribution of neural activity. The circuit formed on Si (111) includes 8×8 pixels of Si probe, two 8-bit shift registers used to select 2D address, and a ripple carry counter for frequency divider. The two shift registers select each pixel of Si probe sequentially. The frequency divider is connected to horizontal scan shift register to control the timing of the scan. If a probe pixel is selected by the scanning circuit, probe voltage is fed to the output through the output stage. At the output stage, a

* Department of Electrical and Electronic Engineering,
Toyohashi University of Technology,
1-1 Hibarigaoka, Tempaku-cho, Toyohashi, Aichi 441-8580

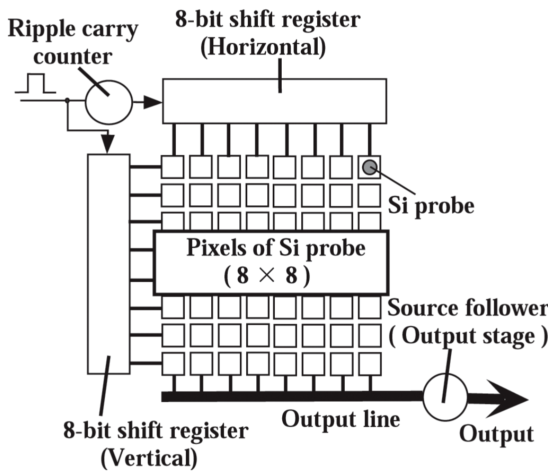


Fig. 2. Configuration of the image-recording circuit.

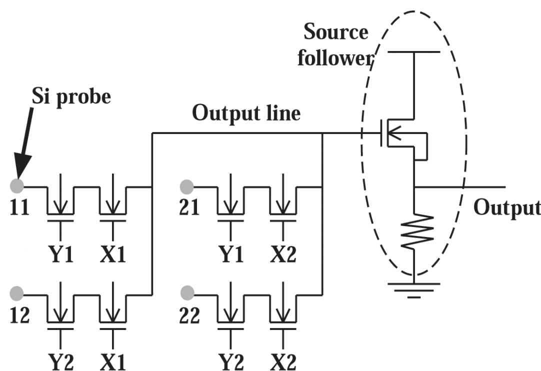


Fig. 3. Diagram of 2×2 signal conditioning circuit for the image-recording sensor of neural activity.

source follower is formed. The high impedance of the neuron is decreased by the source follower in the output stage. Each pixel of the circuit includes one Si probe. The configuration of one pixel with Si probe is shown in Fig.3. In this circuit, a large number of the points can be measured due to the small pixel, because the MOSFETs in one pixel are only two. This circuit was designed and fabricated on Si (111).

As mentioned at introduction, there is a large number of interface state density at Si-SiO_2 interface on Si (111) as compared with that on Si (100). Actually, as a previous result of our fabrication and measurement of n- and p-MOSFET on Si (111), transconductance and mobility of n- and p-MOSFET on Si (111) were smaller than those on Si (100). Transconductances of n- and p-MOSFET on Si (111) were about 65 % and 35% of Si (100) MOSFET, respectively. And mobility of n- and p-MOSFET on Si (111) were about 50 % and 75% of Si (100) MOSFET, respectively. From the results mentioned above, it is understood that those values between Si (111) MOSFET and Si (100) MOSFET are different. Therefore, for fabrication of CMOS circuit on Si (111), the circuit was designed with consideration those differences.

3. Fabrication of CMOS Circuit on Si (111)

There are two problems to be solved for fabrication of CMOS circuit on Si (111) with VLS growth method. One of the problems is the use of Si (111) wafer. On Si (111) wafer, the interface state density is about ten times higher than that on Si (100). It is expected that S-factor will be large and a threshold voltage of MOSFET will be shifted. Another problem in the fabrication process is high-temperature (500 °C ~ 700 °C) damage in the VLS growth process followed after CMOS process. Additionally, Al is impossible to be used in high-temperature VLS process.

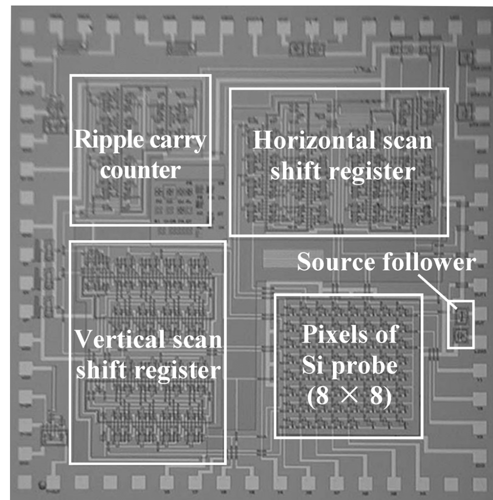


Fig. 4. Photograph of a fabricated chip.
(Chip size: 5.0 mm × 5.0 mm. Design rule: 10 μm rule.).

For the first problem, the fabricated chips were annealed to reduce interface state density by hydrogen ambient (460 °C for 150 min) after CMOS fabrication. In addition, threshold voltages of n- and p-MOSFET were controlled to be 1.0 V and –1.0 V, respectively by optimizing ion-implantation doses. These added processes are considered to be effective for improving characteristics of MOSFET on Si (111). Another problem was solved by changing the interconnection metal material. Instead of Al, tungsten (W) interconnection was used for high-temperature process of VLS growth. The designed CMOS circuit was fabricated on Si (111) wafer at the Electron Device Research Center in Toyohashi University of Technology. Figure 4 shows a photograph of the fabricated CMOS circuit chip on Si (111).

4. Evaluation Results

4.1 Characteristics of MOSFETs on Si (111) As the result of evaluation of I_D-V_G characteristics of n-MOSFET on Si (111) before thermal annealing in hydrogen ambient, threshold voltage, transconductance, field effect mobility, and S-factor were 5.0 V, 6.1 μS, 275 cm^2/V·s and 1540 mV/decade, respectively. Nevertheless, as the result of thermal annealing in hydrogen ambient for 150 min, the threshold voltage, the transconductance, the field effect mobility, and the S-factor were improved to 1.2 V, 9.9 μS, 446 cm^2/V·s and 178 mV/decade, respectively. Figure 5 shows measured I_D-V_G characteristics of n-MOSFET on Si (111) annealed in hydrogen ambient and n-MOSFET on Si (100). The gate length and width are 10 μm and 100 μm, respectively. Threshold voltage, transconductance, field effect mobility, and S-factor of n-MOSFET on Si (100) were 0.8 V, 18.5 μS, 850 cm^2/V·s and 114 mV/decade, respectively.

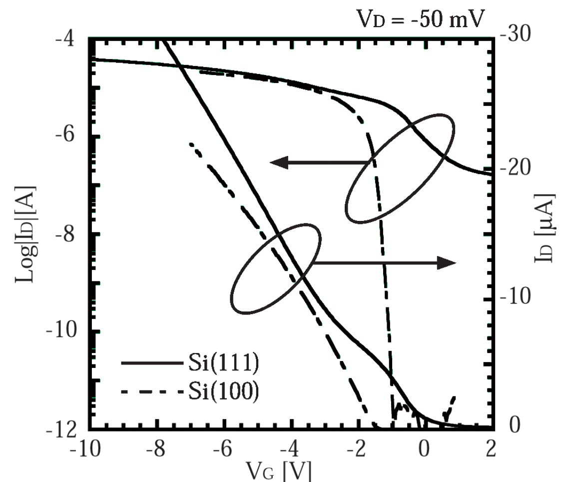
As the result of evaluation of I_D-V_G characteristics of

p-MOSFET on Si (111) before thermal annealing in hydrogen ambient, threshold voltage, transconductance, and field effect mobility were –0.7 V, 3.0 μS and 133 cm^2/V·s, respectively. However, as the result of thermal annealing in hydrogen ambient for 150 min the same as the case of n-MOSFET on Si (111), threshold voltage, transconductance, and field effect mobility were improved to –0.5 V, 4.6 μS and 192 cm^2/V·s, respectively. Figure 6(a) shows measured I_D-V_G characteristics of p-MOSFET on Si (111) annealed in hydrogen ambient and p-MOSFET on Si (100). The gate length and width are 10 μm and 100 μm, respectively. Threshold voltage, transconductance, field effect mobility, and S-factor of p-MOSFET on Si (100) were –1.5 V, 5.3 μS and 232 cm^2/V·s, respectively. The leakage current of p-MOSFET on Si (111) is larger than that of n-MOSFET, because dose density for channel stopper (P) is not enough for p-MOSFET on Si (111). The problem is solved by increasing the ion-implantation dose density for channel stopper. Figure 6(b) shows comparison of measured I_D-V_G characteristics of p-MOSFET on Si (111), for the cases drain voltages are -50 mV and –5 V. When the drain voltage is -50 mV, I_D-V_G characteristic has two kink points. On the other hand, when the drain voltage is -5 V, the kinks in the characteristic are almost invisible. It is necessary to analyze the cause and the phenomenon in detail. However, it is considered that the operation of the circuit is unaffected by the kink in I_D-V_G characteristic, because the drain voltage of the p-MOSFET is high enough to saturate the device.

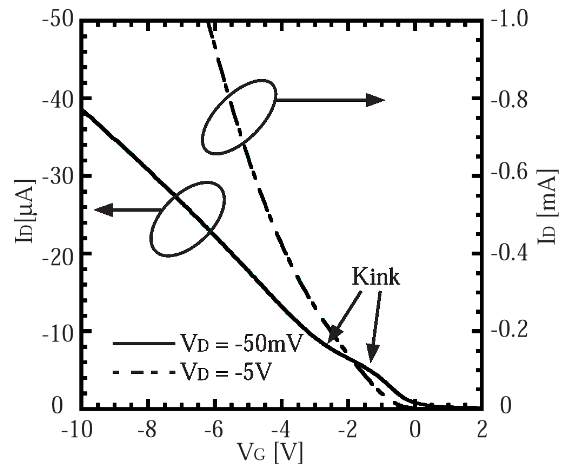
From these results, it is found that hydrogen annealing is very effective for CMOS on Si (111). And as the result of proper ion-implantation dose control, threshold voltages of MOSFET are controlled to the estimated values.

4.2 Operation of the 8-bit Shift register on Si (111)

Figure 7 shows the output waveform of the 8-bit shift register on Si (111). Figure 7(a), (b) and (c) are the clock pulse, the 1st bit output and the 2nd bit output of the 8-bit shift register, respectively. The measured maximum operation frequency of the 8-bit shift register on Si (111) is 3.0 MHz. In that circuit on Si (100), the measured maximum operation frequency is 2.8 MHz. The maximum operation frequency of the circuit on Si (111) is almost equal to that of the circuit on Si (100). One of the reasons of the close maximum operation frequency is the balance of the maximum current of p-MOSFETs and that of n-MOSFETs. From Fig. 5, maximum current of Si (111) n-MOSFET is smaller than that of Si (100). In contrast, from Fig.6 (a), maximum current of Si (111) p-MOSFET is higher than that of Si (100), because the threshold voltage of Si (111) p-MOSFET is lower than that of Si (100).



(a) Si (111) and Si (100).



(b) Drain voltage of Si(111) is changed –50 mV to –5 V.

Fig. 6. I_D-V_G characteristics of p-MOSFET.

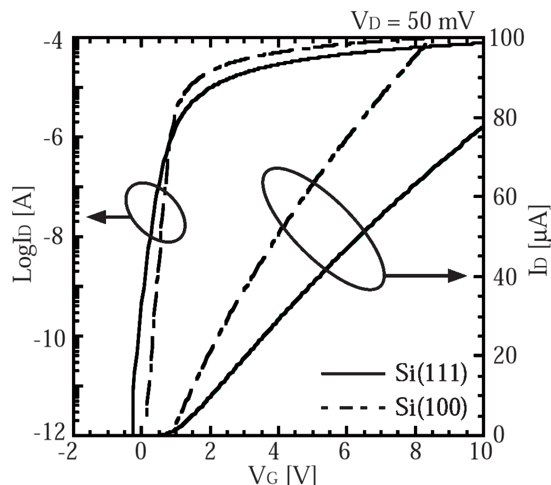


Fig. 5. I_D-V_G characteristics of n-MOSFET on Si (111) and Si (100).

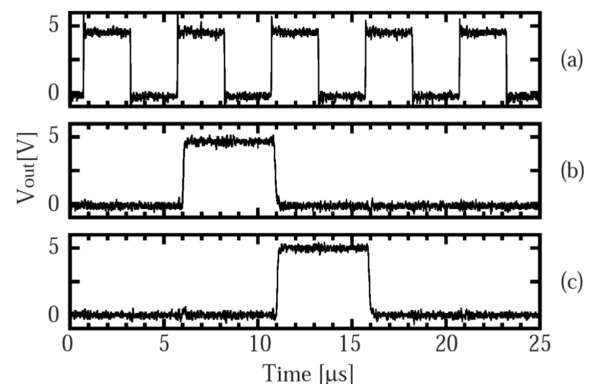


Fig. 7. Output voltage of the 8-bit shift register on Si (111). (a) Clock pulse. (b) 1st bit output. (c) 2nd bit output.

The bandwidth of neural activity signal is below 10 kHz. Then, each probe pixel has to be switched at a 1.2 MHz to scan 64 sites. So, the operation speed is high enough to obtain a potential image from this device at the required frame rate. If a higher scan speed is required, design rule shrinking of CMOS circuit is necessary.

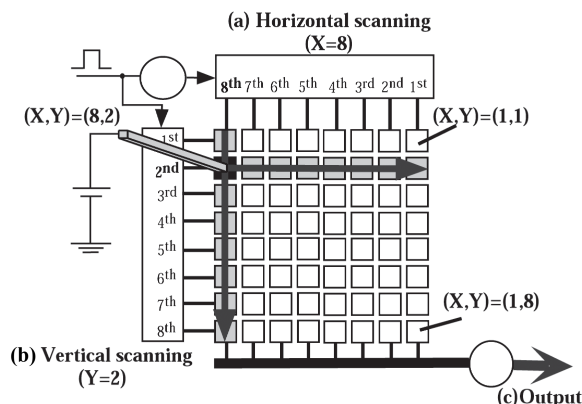


Fig. 8. Diagram of the way to evaluate the image-recording circuit for neural activity.

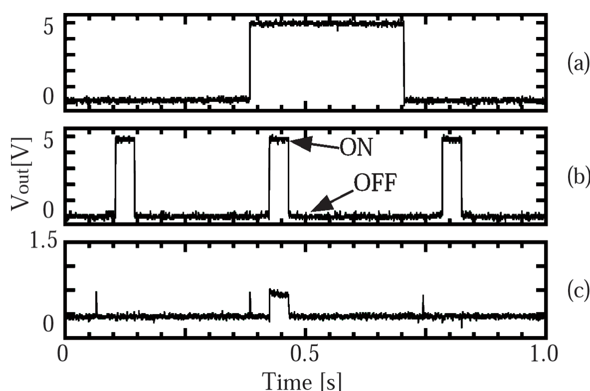


Fig. 9. Output voltage of the Integrated Circuit on Si (111) for image recording of neural activity, when (X, Y) = (8, 2) was selected to apply potential. (a) Output of 8th bit of the horizontal scanning circuit. (b) Output of 2nd bit of the vertical scanning circuit. (c) Output from the output line.

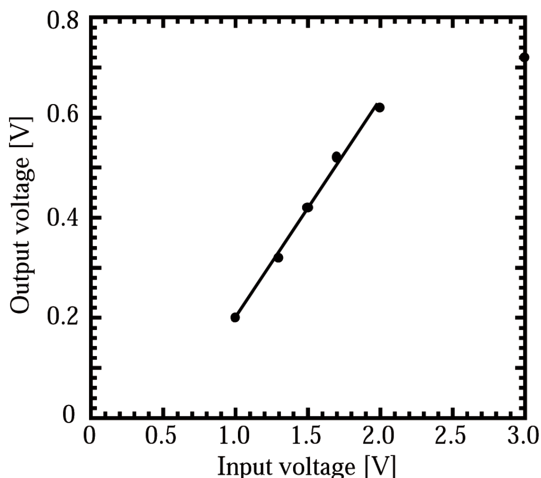


Fig. 10. Input-output characteristic of the pixel.

4.3 Operation of the Image-Recording Circuit for Neural Activity The image-recording circuit of neural activity on Si (111) was evaluated with external voltage. The pixel at (X, Y) = (8, 2) was selected to apply a potential externally as shown in Fig.8.

The output of 8th bit of the horizontal scanning circuit and the output of 2nd bit of the vertical scanning circuit are shown in Fig.9 (a) and (b), respectively. The period of horizontal scanning circuit is 8 times as long as that of vertical scanning circuit. When the pixel is selected, the potential of each pixel is fed to the output line. The output of (X, Y) = (8, 2) pixel appeared at 0.425 sec selectively in Fig.9(c). This output corresponds to a logical "AND" of the select signals shown in Fig.9 (a) and (b). Therefore, it is confirmed that the address scanning circuit in the fabricated chip selects each pixel.

Then, pixel output characteristic for the external applied voltage from 1 V to 3 V are evaluated. The input-output characteristic is shown in Fig.10. For an applied voltage between 1.0 V and 2.0 V, the output voltage change is proportional to the input voltage of the selected pixel. The output voltage is saturated when the external voltage is more than 2.0 V. The amplitude of neural activity voltage is in a range from a few mV to 100 mV. And if the circuit is biased, the pixel is able to measure around 0 V. Therefore, it is inferred that the pixel can be used to measure the neural activity voltage.

From these results, it is considered that CMOS signal processing circuit for neural activity with VLS grown Si probe can be realized by CMOS technology on Si (111).

5. Conclusion

CMOS Integrated Circuit for image-recording sensor of neural activity is fabricated on Si (111). It is found that CMOS circuit on Si (111) can be fabricated with enough performance by adjusting some fabrication process parameters such as ion-implantation dose and annealing time in hydrogen ambient. The operation of scanning circuit on Si (111) is confirmed. The signal bandwidth of the circuit is nearly equal to that of the scanning circuit fabricated on Si (100). And the measured signal bandwidth is enough for the purpose of neural activity recording. A linear relationship between input and output of the detection circuit for each pixel is obtained. It is experimentally demonstrated that CMOS circuits on Si (111) have close performance to CMOS circuits formed on Si (100).

Acknowledgments

This work was supported in The 21st Century COE Program "Intelligent Human Sensing" and a Grant-in-Aid for Scientific Research from the ministry of Education, Culture, Sports, Science and Technology Japan.

(Manuscript received December 13,2002, revised March 12,2003)

References

(1) M.D.Gingerrich and K.D.Wise : "An active microelectrode array for multipoint stimulation and recording in the central nervous system", Proc. the 10th Int. Conf. on Solid-State Sensors and Actuators (Tranceducer'99), pp.280-283, Sendai, Japan (1999)

(2) K.E. Jones, P.K. Campbell, and R.A. Norman : "A glass/silicon composite intracortical electrode array", *Ann. Biomed. Eng.*, **20**, pp.423-437 (1992)

(3) W.L.C. Rutten, J.P.A. Smit, T.A. Frieswijk, J.A. Bielen, A.L.H. Brouwer, J.R. Buitenweg, and C. Hedia : "Neuro-electrode interfacing with multielectrode arrays", *IEEE Eng. Med. Biol.*, **18**(3), pp.47-55 (1999)

(4) R.A.Norman: "Visual neuroprostetics functional vision for the blind", *IEEE Eng. Med. Biol*. **14**(1), pp.77-83 (1995)

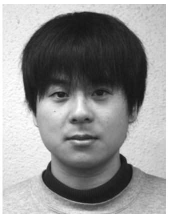
(5) M. Ishida, K. Sogawa, A. Ishikawa, and M. Fujii: "Selective growth of Si wire for intelligent nerve potential sensors using vapor-liquid-solid growth", Proc. the 10th Int. Conf. on Solid-State Sensors and Actuators (Tranceducer'99), pp.866-869, Sendai, Japan (1999)

(6) R.S.Wagner and W.C.Ellis "Vapor-Liquid-Solid Mechanism of Single Crystal Growth." *Appl. Phys Letters*, Vol.4, No.5, pp.89-90 (1964)

Yoshiko Kato (Member) was born in Chiba, Japan, on October 28, 1977. She received the B.S. degree in 2000 and the M.S. degree in 2002, in Electrical and Electronic Engineering from Toyohashi University of Technology, Aichi, Japan. She is currently working on CMOS integrated circuits, simulation and imaging system for neural activity. She is a member of Japan Society of Applied Physics.

Takeshi Kawano (Member) was born in Yamaguchi, Japan, on July 23, 1976. He received the B.S. degree in 1999 and the M.S. degree in 2001, in Electrical and Electronic Engineering from Toyohashi University of Technology, Aichi, Japan. He is currently working on micro-probe array by selective Si epitaxital growth, evaluation and monolithic IC process for smart neural recording sensor systems. He is a member of Japan Society of Applied Physics.

Yoshiaki Ito (Non-member) was born in Shizuoka, on April 2, 1978. He received the B.S. degree in Electrical and Electronic Engineering from Toyohashi University of Technology, Aichi, Japan, in 2001. He is currently working on formation and characterization of low noise fully differential amplifier.



Hidekuni Takao (Member) was born in Kagawa, Japan, in 1970. He graduated Takamatsu National College of Technology, Takamatsu, Japan in 1991. He received his B.E. and M.E. degree in electrical and electronic engineering in 1993 and 1995, respectively, and received his Ph.D. degree in electronic and information engineering in 1998, all from Toyohashi University of Technology, Aichi, Japan. He was a postdoctoral research fellow of Japan Society of the Promotion of Science (JSPS) from 1998 to 1999. Since 1999, he has been a research associate of the department of electrical and electronic engineering in Toyohashi University of Technology. He is currently working on micro fluidic devices for micro total analysis systems (μTAS), CMOS smart mechanical sensors using MEMS technology, and SOI sensor systems for severe environments.

Kazuaki Sawada (Member) was born in Kumamoto, Japan in 1963. He received his B.A. degree and M.S. degree in electrical and electronic engineering and Dr. Eng degree in system and information engineering all from Toyohashi University of Technology in 1986, 1988 and 1991, respectively. From 1991 to 1998, he was at the Research Institute of Electronics, Shizuoka University, where he was serving as Research Associate. Since 1998, he has been at the Department of Electrical and Electronic Engineering, Toyohashi University of Technology, where he is now serving as Associate Professor. His current research interest is focused on the ultrahigh-sensitive image device using field emitter arrays and amorphous silicon avalanche photo-diode films.

Makoto Ishida (Member) was born in Hyogo, Japan, in 1950. He received the PhD degree in Electronics Engineering from Kyoto University, Kyoto, Japan, in 1979. Since 1979, he has been at Toyohashi University of Technology, and he is a professor of Electrical and Electronic Engineering. He is working on smart microchip with epitaxial Si probe, heteroepitaxial growth and processes of SOI material including epitaxial Al_2O_3 insulator and Si, and their device applications including sensor and IC in electron device research center in Toyohashi University of Technology.