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Fabrication and properties of ultrasmall Si wire arrays with circuits by vapor–liquid–solid growth☆

Takeshi Kawano*, Yoshiko Kato, Masato Futagawa, Hidekuni Takao, Kazuaki Sawada, Makoto Ishida

Department of Electrical and Electronic Engineering, Toyohashi University of Technology, 1-1 Hibarigaoka, Tempaku-cho, Toyohashi 441-8580, Japan

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Abstract

A micro-Si wire probe array chip with on-chip circuits has been developed for the applications on multichannel electrodes of neuroelectronic interface systems. Selective Au–Si_2H_6 vapor–liquid–solid (VLS) growth method provides a successful Si probe array on Si(1 1 1) wafers in predetermined positions and probe sizes. Si probes with 160 μm in length and 3.5 μm in diameter at tip were grown for 2 h at 700 °C. Moreover, the circular cone type shape of the Si probes was controlled by changing the Si_2H_6 gas pressures in the VLS growth. After wiring process for on-chip circuits on Si(1 1 1) wafers, the Si probes were grown perpendicular to the wafer surface by the VLS growth process. Conductivity of Si probes was controlled by using phosphorous diffusion, resulting in a resistivity of $10^{-2}\ \Omega \cdot \mathrm{cm}$ from $10^{4}\ \Omega \cdot \mathrm{cm}$ at a diffusion temperature of 1100 °C. In in vivo studies, penetrating micro-probe array with low impedance such as the VLS grown Si probes has been desired. Using the VLS grown Si probes, these electrical signals was detected successfully. © 2002 Elsevier Science B.V. All rights reserved.

Keywords: Smart neural activity recording sensor; Penetrating type electrode array; Vapor–liquid–solid growth; Micro-Si probe array chip; Neural interface

1. Introduction

In in vivo studies, multipoint recordable penetrating probes with the same size as the neurons allow researchers to reconsider the neural systems [2–5]. For this field, we have proposed penetrating micro-Si wire probe array with on-chip signal-processing circuitry using selective vapor–liquid–solid (VLS) growth method and integrated circuit (IC) process on Si(1 1 1) substrate [6]. Using a SiO_2 window mask and lift-off method of photolithographic techniques, the Si probe array in the VLS growth was fabricated with the spacing and the diameter controlled in a few microns. The on-chip processing circuitry has no external wiring connections between the sensing sites and amplifiers; therefore a very small sensor size is realized. The best way to record neural activity electrical potentials is by using an on-chip integrated circuitry with addressed-accessing and amplifiers. Such a structure of on-chip active electrodes can be expected to be an ideal electrode array technology in neuroscience field to applications for recording retinal cell electrical potentials and/or studying of space sickness in a micro-gravity environment. Moreover, properties of the Si probe array chip can be inserted into neural tissue and applied for stimulation to achieve the neuroprosthetics.

It is well known that growth direction of the Si wire probe is ⟨1 1 1⟩ in the VLS growth, and Au dots on the Si wafer become Au–Si alloy droplets and remain at the tips of Si probes during the VLS growth, which resulted in a high aspect ratio of Si probes [7,8]. The growth mechanism showed that the Si probes on the Si wafer was more than 1 mm in length with a few microns in the probe diameter. For a few technologies using the VLS growth, the Si probes have been fabricated for IC testing probe cards [9]. In recording neurons in the brain, to penetrate through the surface and reach the normal neuronal input on the visual cortex in humans, penetrating electrode must have a length of a few millimeters [5].

Fig. 1 illustrates the schematic overview of micro-Si wire probe sites in neural activity recording chip. Neural activity electric potentials are recorded through the tips of the penetrating Si probe array with neuron size in diameter and spacing. Each Si probe in the array can be linked to on-chip integrated amplifiers using an addressed-accessing circuitry. The chip design provides researchers a high-resolution of neural activities distribution below the cortical surface.

☆ All the significant results have already been published in the technical digest [1].

* Corresponding author. Tel.: +81-532-44-6745; fax: +81-532-44-6757.
E-mail address: kawano@icg.dev.eee.tut.ac.jp (T. Kawano).

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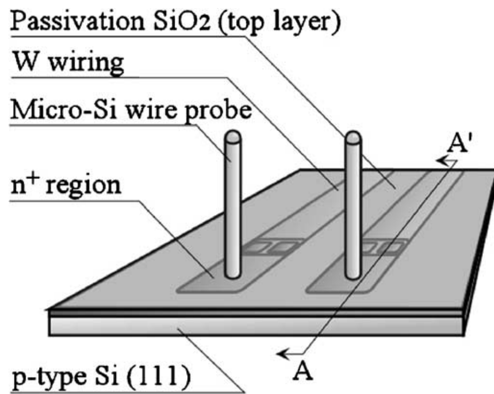


Fig. 1. Schematic overview of micro-Si wire probe sites in neural activity recording chip.

Fabrication techniques and characterization of the Si wire probe arrays with on-chip circuits are described in this paper, which focuses on the improved VLS conditions for the high growth rates of the Si probes. And lower growth temperature which results in decrease of the damage to on-chip MOSFET's circuitry was also studied. The Si probe showed a circular cone shape that depended on the growth gas pressures. The reduction of the Si probe impedance is studied by phosphorous diffusion, which is suitable for fabrication processes for this smart chip. Electrical evaluation of the probes is done using simulated neural activity electric potentials.

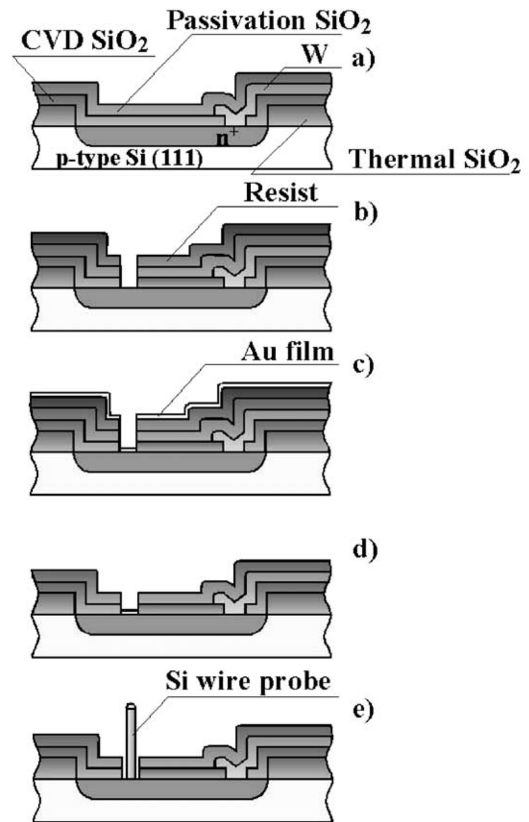


Fig. 2. Process sequence for Si wire probe chip with W wiring circuits through section AA′ in Fig. 1: (a) passivation SiO_2 (600 nm); (b) patterning (BHF); (c) Au evaporation (Au film 160 nm); lift-off (acetone dip); (e) VLS growth (temperature 500–700 °C).

2. Fabrication of Si wire probe chip

A Si(1 1 1) wafer was used in the Si wire probe array chip, because the probes can be grown perpendicular to the Si(1 1 1) surface in the VLS growth. Epitaxial Si probes were grown at a pre-determined position, where Au dot arrays were formed by SiO_2 window mask and Au lift-off method after Si standard MOSFET's process. Fig. 2 illustrates the process sequence for the Si probe chip through the section AA′ in Fig. 1. In the first step of the process, thermal SiO_2 was grown on p-type Si(1 1 1) wafer, and the SiO_2 layer on active region was removed. The active region was doped heavily with n-type dopant, and then a SiO_2 layer was deposited again by CVD. After etching the CVD SiO_2 layer, W wiring was formed for subsequent high temperature process. The W wiring layer must be covered by a passivation layer in a corrosive environment such as the brain. The passivation layer was formed in a 600 nm thick SiO_2 layer over the W wiring (Fig. 2a).

In the VLS growth after the IC process, the passivation layer and the CVD SiO_2 layer were used as a SiO_2 window mask and a Au layer with thickness of 160 nm was evaporated after patterning of SiO_2 window mask. After Au lift-off, patterned Au dots remained at the Si probe sites in a determined position (Fig. 2b–d). Then the sample was introduced immediately into a gas source molecular beam epitaxy (GS-MBE) chamber. In this chamber, after heating the Si substrate to form Au–Si alloy droplets above Au–Si eutectic point, the VLS growth was carried out. After the process, Si probe crystals were obtained on the Au dot sites. The VLS growth conditions, the probe shapes and conductivity were described in detail after this section.

Due to the VLS growth, the poly-Si growth occurred at other areas except the Si wire probe sites. This poly-Si layer was successfully removed by a reactive ion etching (RIE) process using SF_6/O_2 plasma, so that the Si probes can be electrically isolated from each other (Fig. 2e). To characterize electrical properties of the Si probes, the passivation SiO_2 layer on the connecting W pad was selectively patterned and etched.

The process for the micro-Si wire probe array on Si wafer is simple as described above. Using this growth technology, a high aspect ratio of the probes is obtained and its probe array is capable of integration with the on-chip signal-processing circuitry [6], which means that this electrode technology will yield several advantages for the neuroscience field.

3. Penetrating Si VLS growth

The Si wire probe length in neuroscience depends on various applications and varies from a few microns to a few

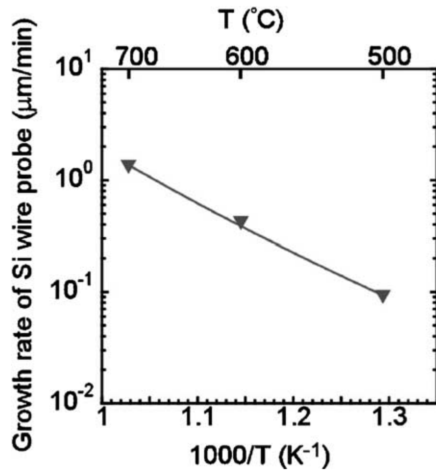


Fig. 3. Growth rates of Si wire probes as a function of growth temperatures.

millimeters. For example, the Si probe which is a few millimeters in length is used to penetrate through the cortical surface and down to the level of the normal neuronal input to the visual cortex [5]. In the Si VLS growth, the growth rate depends on the total number of Si atoms that reached the surface of the Si substrate. The growth rate has been controlled using various growth temperatures and gas pressures.

The Si wire probe growth was done in a Si_2H_6 GS-MBE chamber. The pressure in the growth chamber was in the range of 10^{-7} Pa. The wafer can be heated from the back using a carbon heater with temperature rising to 900 °C, and Si_2H_6 gas was introduced to the wafer surface at a pressure between 5×10^{-2} and 1×10^{-5} Pa. In order to increase the growth rate, the introduced flow of Si_2H_6 gas into the chamber was increased. Fig. 3 shows the growth rate of the Si probe as a function of the growth temperatures from 500 to 700 °C under the growth Si_2H_6 gas pressure of 7×10^{-3} Pa. In the Si probe growth, the selective VLS growth method was used to control the Au dots positions diameter using SiO_2 window mask and lift-off method before the Si probe growth.

Fig. 4 shows a scanning electron microscope (SEM) micrograph of the grown Si wire probes of a 2×2 array with 160 μm in length and 3.5 μm in diameter at tip. The growth temperature was 700 °C and the growth time was 2 h. The probe size was determined from the SEM micrograph, and we estimated that a growth rate of 1.3 μm/min was obtained, which was 10 times larger than 0.1 μm/min at a growth temperature of 700 °C, as described in a previous paper [6]. From the SEM micrograph, we note that these Si probes' shape was like a circular cone. In penetrating experiments to record neural activity potentials, this shape is suitable for penetration into neuron cells through the cortex, without the probe breaking or curving, which causes errors in recording points. The circular cone type is due to the

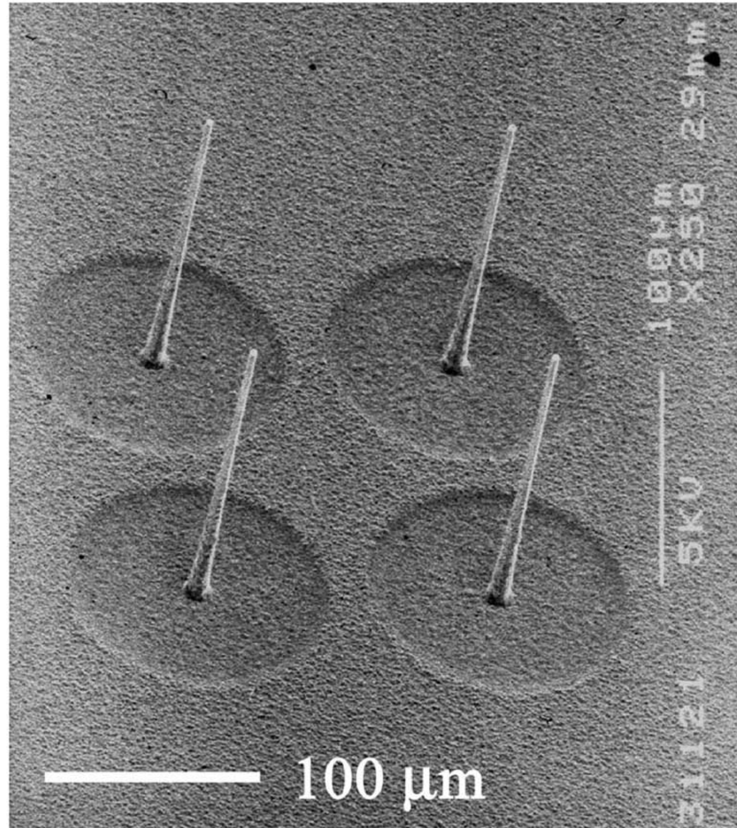


Fig. 4. Selective Si wire probes of a 2×2 array 160 μm in length and 3.5 μm in diameter at tips realized with SiO_2 window mask and lift-off process. The VLS growth was done at 700 °C for 2 h.

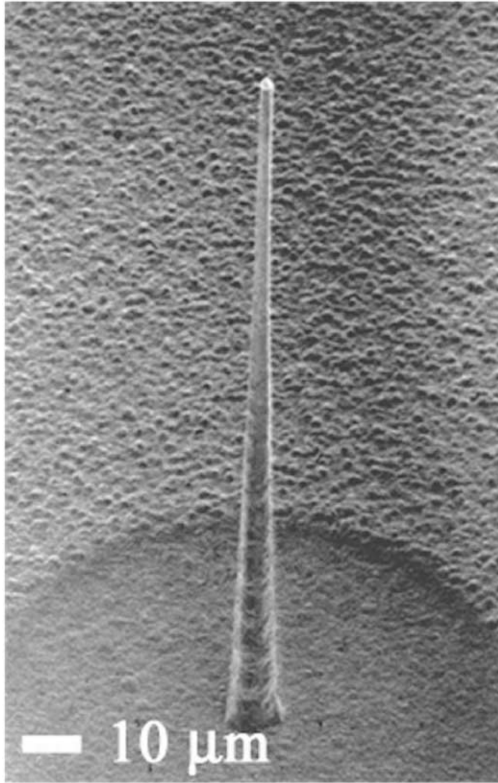


Fig. 5. Circular cone type of Si wire probe was grown in VLS growth. Si probe diameters of the tip and bottom were 3.5 and 10 μm, respectively.

allowed Si growth at the sidewall of the probe. The Si probe diameters of the tip and the bottom were 3.5 and 10 μm, respectively, as shown in Fig. 5.

Fig. 6 shows the results of the Si wire probes for different Si_2H_6 gas pressures. To control the taper of the circular cone shape of the probes, the Si_2H_6 gas pressure was changed to increase the Si growth rate at the sidewall of the probes. The Si probes were grown at a temperature of 700 °C at a fixed growth time of 2 h. Under this condition, the Si_2H_6 gas pressure was changed from 7×10^{-3} to 1×10^{-2} Pa. The diameter sizes of the Si probes were obtained from SEM micrographs. In Fig. 6, the Si probe diameter was plotted from the bottom to the tip. The bottom diameter of the Si probe grown at a gas pressure of 1×10^{-2} Pa was doubled at a grown pressure of 7×10^{-3} Pa, while the Si probe tips had almost the same diameter. It means that the probe's shape can be controlled by changing the gas pressure, which allows us to fabricate suitably the shape for various Si probe applications.

The smart Si probe chip must be with on-chip signal-processing circuitry on Si(1 1 1) wafer. However, the circuits may have the effects of Au diffusion after the VLS growth process. Electrical characteristics of n-type MOSFETs on Si(1 1 1) were also studied [7]. After the VLS process, n-type MOSFETs showed no large change in the threshold voltage and leakage current compared with those before the VLS growth. The characteristics are enough to fabricate the Si probe array on circuitry on Si(1 1 1) wafer directly. These experimental results in the details will be published in the near future.

4. Electrical properties

Fig. 7 shows the photograph of Si wire probe's sites of the chip fabricated using the fabrication process described in Fig. 2. In this design, probes with W wiring circuits were spaced 100 μm of each other. Fig. 8 shows SEM views of the Si probe site in Fig. 7. The Si probe was grown with 30 μm in length and 2 μm in diameter at a growth temperature of 600 °C for 30 min under a Si_2H_6 gas pressure of 7×10^{-3} Pa. Firstly, for the Si probe grown without impurity doping process, current–voltage measurements of the probes showed a linear characteristic and a resistivity of $10^4\ \Omega \cdot cm$. In the measurement of the Si probe, a system that can be manipulated with sharpened W electrode in a few microns was used to contact the tip of the Si probe. And the contact resistance was not a problem due to Au–Si alloy tips as shown in Fig. 5. For recording of low potential levels such as electrical potential of neuron activity, low impedance Si probes are desired. In order to get a well-conducting char-

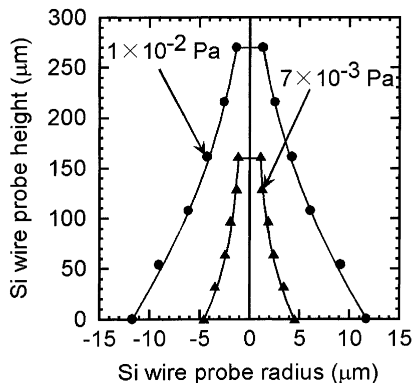


Fig. 6. Shape of the circular cone Si wire probes for two growth Si_2H_6 gas pressures of 1×10^{-2} and 7×10^{-3} Pa.

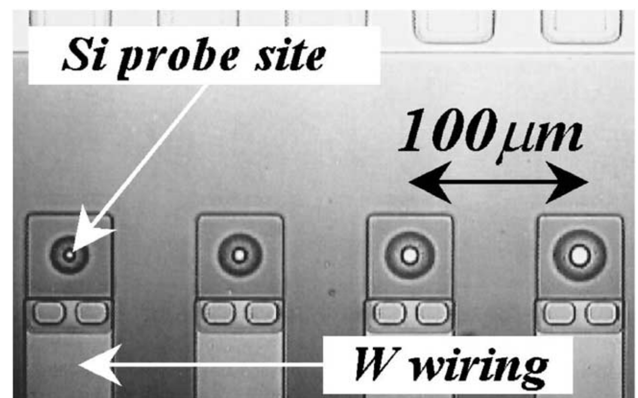
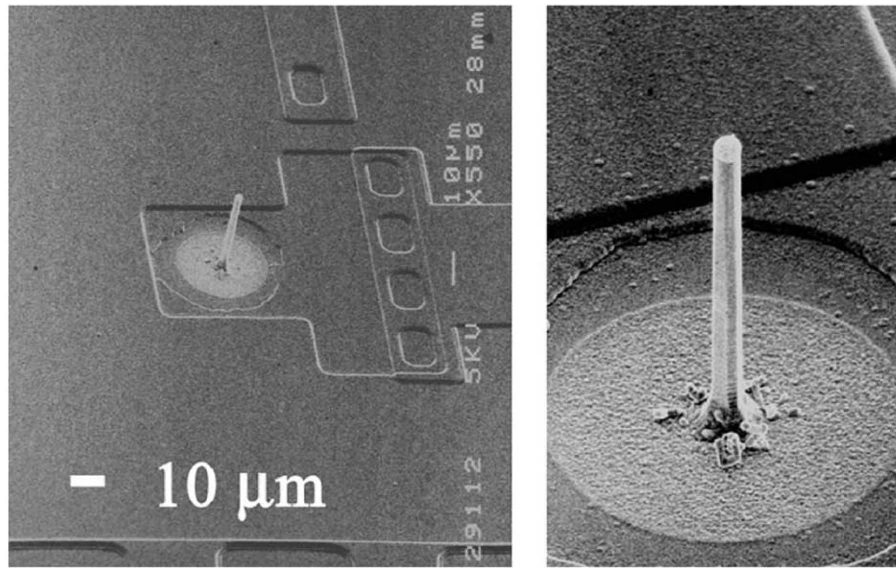


Fig. 7. Photograph of Si wire probe sites in the array chip. The Si wire probes with W wiring circuits were spaced 100 μm of each other.



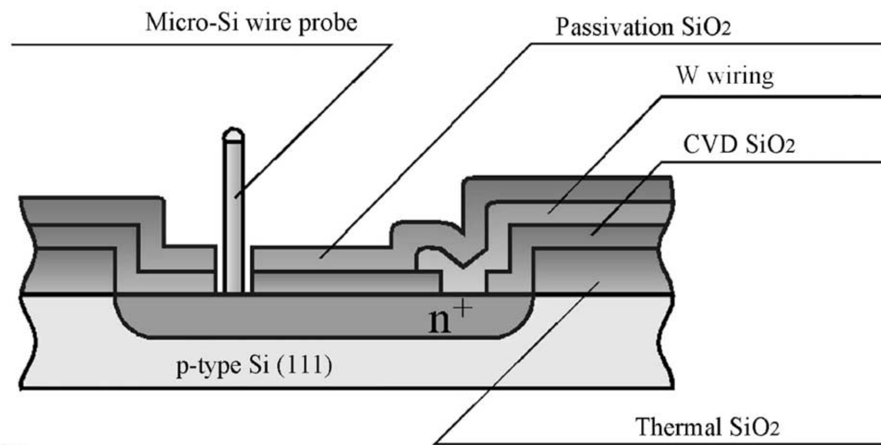


Fig. 8. The Si wire probe on Si(1 1 1) with W wiring circuits: (a) SEM views of Si wire probe 30 μm in length and 2 μm in diameter at a growth temperature of 600 °C for 30 min; (b) schematic diagram of Si probe.

acteristic of these electrodes with three-dimensional structure, metal coating process was reported [4,9]. On the other hand, we propose that impurity diffusion technique is more useful to get conductive Si probes with a few micron space and high aspect ratio.

Fig. 9 shows the resistance and resistivity of the Si wire probes as a function of the radius after the phosphorous diffusion at 1100 °C. Under this diffusion condition, the whole of the Si probe with diameters ranging from 2.3 to 3.5 μm was heavily doped with phosphorous. After the phosphorous diffusion, the Si probes showed a resistivity of $10^{-2}\ \Omega \cdot cm$. The value was estimated from the size and the resistance of the Si probe. The resistance of the Si probe with 3.5 μm in diameter and 10 μm in length was 77 Ω. This is enough resistance so that the Si probe can be used in the applications mentioned above. Lower diffusion temperatures can be used, since the phosphorous diffused at the

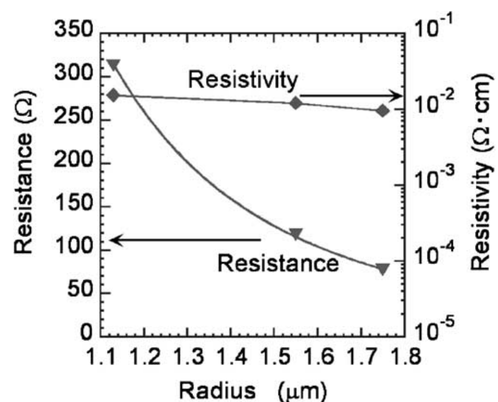


Fig. 9. Electrical properties of Si wire probe after phosphorous diffusion at 1100 °C. The Si probes were 2.3–3.5 μm in diameter and typically 10 μm in length.

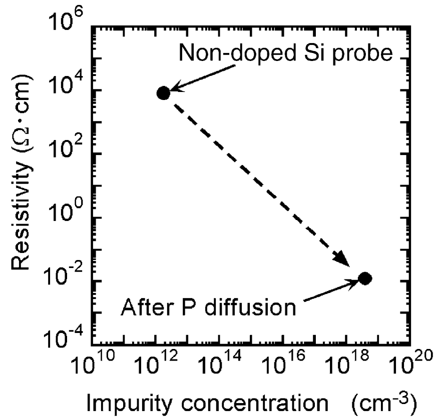


Fig. 10. Resistivity and impurity concentration of Si wire probe both before and after phosphorous diffusion to the probe at 1100 °C.

sidewall of the probe allows us to get conductive Si probes. For penetration experiments, these Si probes must be encapsulated with insulating layer at the sidewall, except the probe tips. Fig. 10 shows the relationship between resistivity and impurity concentration of both non-doped and phosphorous-doped Si probes in this work.

5. Neural activity experiment

The Si wire probes with on-chip circuits were evaluated using a simulated stimulation signal of neural activity, using the same manipulable system as measurement of the probe current–voltage characteristics. Fig. 11 shows results of the simulated neural activity potential recording, where a signal with potential of 10 mV and frequency of 10 kHz led to a Si probe's tip. The evaluated Si probe was 1.9 μm in diameter and 21.4 μm in length. And the probe was diffused at 1040 °C, which was resistance of 5 kΩ. The response of above described stimulation signal through the Si probe showed no reduction of input signal amplitude, and output signal followed the input signal. From the experimental results, it was found that the Si probes are useful electrodes for recording neural activity potentials.

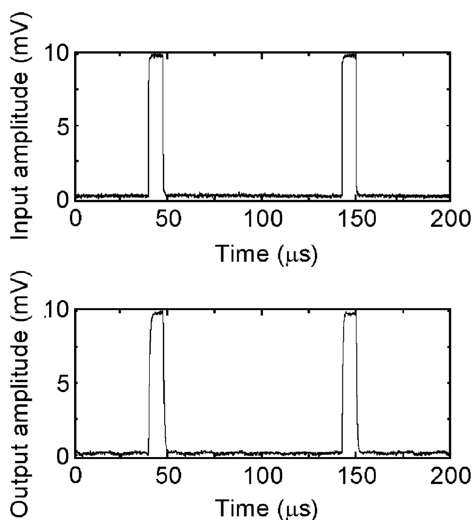


Fig. 11. Signals recorded with Si wire probe chip. Input signals of activity model with 10 mV potential at 10 kHz and output response through the Si probe with W wiring.

6. Conclusions

The micro-Si wire probe array chip has been presented for multipoint recording of neural activity potentials. In the fabrication process, the key technology is the selective VLS growth method. The fabrication technique provides us Si probes with the same size as the neurons and high aspect ratio for penetrating. Moreover, the technology allows the probes with on-chip circuitry of addressed-accessing and amplifiers. For recording the distribution of the neural activity potentials, these circuits will operate the arrayed probes at the same recording time. In order to realize the fabrication of Si probe array, Si(1 1 1) substrate was used and n-type MOSFETs were also fabricated on the same Si(1 1 1) wafer. As shown in our previous report [6], n-type MOSFETs can be also fabricated on Si(1 1 1) instead of Si(1 0 0) substrates without serious changes on n-type MOSFET's characteristic.

This work described the selective Si VLS growth and IC process on Si(1 1 1), and also the electrical properties of the VLS grown probes. W wiring, passivation SiO_2 layer and poly-Si etching were used for the Si probes with on-chip circuitry, suitable for recording of neural activity potentials. In the Si probe growth, increased Si_2H_6 gas flow conditions were used, and a growth rate of 1.3 μm/min was obtained at 700 °C. Grown Si probes showed the shape of a circular cone, that taper was controlled using changing Si_2H_6 gas pressures in the growth process. The probe taper was suitable for penetration experiments. Resistivity of Si probes was high, without the doping process. But Si probe resistance was reduced by the phosphorus diffusion technique. Using this Si probe, the ability of recording neural activity potentials was evaluated, and it was found that these Si probes are very useful in neuroscience.

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Biographies

Takeshi Kawano was born in Yamaguchi, Japan, in 1976. He received the MS degree in electrical and electronic engineering from Toyohashi University of Technology, Aichi, Japan, in 2001. He is currently working on micro-probe array chip by selective Si epitaxial growth, evaluation and monolithic IC process for smart neural recording sensor systems.

Yoshiko Kato was born in Chiba, Japan, in 1977. She received the BS degree in electrical and electronic engineering from Toyohashi University of Technology, Aichi, Japan, in 2000. She is currently working on CMOS integrated circuits, simulation and imaging system for neural activity recording.

Masato Futagawa was born in Kagawa, Japan, in 1977. He received the BS degree in electrical and electronic engineering from Toyohashi University of Technology, Aichi, Japan, in 2000. He is currently working on Si probe growth, design and fabrication for various the Si probe fields.

Hidekuni Takao was born in Kagawa, Japan, in 1970. He received the BE and PhD degrees in electrical and electronic engineering from Toyohashi University of Technology in 1993 and 1998, respectively. He worked at Toyohashi University of Technology in 1998 as a post-doctoral fellow supported by the Japan Society of the Promotion of Science for 1 year. Since April 1999, he has been a research associate of Toyohashi University of Technology. He is currently working on CMOS integrated sensor systems for high temperature environments.

Kazuaki Sawada was born in Kumamoto, Japan, in 1963. He received the Dr. Eng. degree in system and information engineering from Toyohashi University of Technology, Aichi, Japan, in 1991. From 1991 to 1998, he was a research associate at the Research Institute of Electronics, Shizuoka University. Since 1998, he is at the Department of Electrical and Electronic Engineering, Toyohashi University of Technology, where he is now serving as an assistant professor. His current research interest is focused on the ultrahigh sensitive image device using field emitter arrays and amorphous silicon avalanche photodiode films.

Makoto Ishida was born in Hyogo, Japan, in 1950. He received the PhD degree in electronic engineering from Kyoto University, Kyoto, Japan, in 1979. Since 1979, he has been at Toyohashi University of Technology, and he is a professor of electrical and electronic engineering. He is working on smart microchip with epitaxial Si probe, heteroepitaxial growth and processes of SOI material including epitaxial Al_2O_3 insulator and Si, and their device applications including sensor and IC in electron device research center in Toyohashi University of Technology.